High-Performance Non-Volatile Memory

1992

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Printed in U. S. A.

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General Information

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363.

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Company Profile

Company Description

WSI is a market leading producer of high-performance field-programmable peripheral integrated circuits. The company was founded in 1983 to serve the needs of system designers who are required to reduce the size and power consumption of their systems, achieve higher system performance, and shorten their product development time in order to achieve faster market entry.

WSI produces a family of field-programmable microcontroller peripherals as well as a broad line of high-performance non-volatile PROM and EPROM memory products, all based on its patented self-aligned split-gate CMOS EPROM technology. The new programmable microcontroller peripherals enable rapid system design of smaller, more efficient high-performance embedded controllers. These devices are the first to integrate high-performance EPROM, SRAM and user-configurable logic and deliver a performance and integration breakthrough to the programmable peripherals market.

WSI's technology and product lines have enabled the company to establish itself as a leading supplier of high-performance programmable solutions to a broad customer base that includes some of the world's largest and most technologically advanced electronics companies.

Technology

WSI's patented self-aligned, split-gate EPROM technology enables higher performance and greater memory densities per chip area than the traditional stacked-gate method. By developing significantly higher read current, the WSI EPROM cell has enabled the development of several memory devices that are the fastest of their type on the market. This core NVM technology is further leveraged by WSI's architecture and design innovations such as Alternate Metalless Ground (AMG) and contactless memory arrays resulting in dramatic die area savings. This high density memory capability enables WSI to provide cost-effective market leading products. WSI's proprietary NVM technology (licensed to Sharp Corporation, National Semiconductor Corporation and Advanced Micro Devices) has enabled WSI to be first in the industry with numerous product breakthroughs in speed, high density, process innovations and packaging.

Markets and Applications

WSI's Programmable Microcontroller Peripheral and high-performance non-volatile memory products are used by the world's leading suppliers of advanced electronic systems in telecommunications, data processing, military, automotive and industrial markets.

Applications for the Programmable Microcontroller Peripherals include cellular telephones, disk drive controllers, modems, bus controllers, engine management computers, telecom switchers, motor controllers and others. High performance memory applications include digital signal processing, engineering workstations, high-speed modems, video graphics controllers, radar and others. By virtue of their high speed and programming capability, WSI products are ideally suited for these applications where designers are pushing the limits of system performance in highly competitive markets.

Product Groups

Programmable Microcontroller Peripherals

WSI's family of Programmable Microcontroller Peripherals represents a new class of programmable products. They enable system designers to reduce the size of their products, achieve lower operating power, optimize system performance and shorten product development cycles. They are the first field-programmable devices to integrate high-speed EPROM, SRAM and programmable logic on a single chip. The Programmable Microcontroller Peripherals include the 6 member PSD3XX family, and the MAP168.

PSD3XX Family: Microcontroller Peripherals with Memory

Each member of the PSD3XX family is a single-chip, field-programmable circuit that integrates all the required peripheral memory and logic elements for an embedded-control design. Programmable logic, page logic, programmable I/O ports, busses, address mapping, port address/data tracking, 256K to 1 Mb EPROM, and 16K SRAM are all on board. Advanced features such as memory paging, microcontroller port reconstruction, track mode, configuration security bit, and cascading further enhance the utility and value of the PSD3XX family. PSD3XX family devices are ideal for applications requiring high-performance, low power and very small form factors such as fixed disk control, cellular telephones, modems, computer peripherals, and automotive and military applications.

PSD101 DSP Peripheral with Memory

Similar to the PSD3XX family, the high speed PSD101 integrates high-performance EPROM, SRAM, a PAD and user-configurable logic. Ideal for high-speed applications requiring expanded memory, system integration and increased data security, the 45 ns PSD101 is used with high speed digital signal processors, microprocessors and microcontrollers.

PAC1000 Programmable Peripheral Controller

The high speed PAC1000 sets a new standard for Programmable Peripheral performance, integration and functionality. The PAC1000 replaces up to 50 complex devices in high-end embedded controllers and microprocessor-based systems. Combining a CPU, 1K x 64 EPROM and extensive user-configurable logic, the PAC1000 assists its host processor with high rates of data manipulation and control, freeing the processor for other system functions. The 16 MHz PAC1000 has been designed into numerous high-performance applications such as work-station direct memory access controllers, video imaging digital signal processors, and VME bus LAN controllers.

Programmable Peripheral Development Tools

WSI's Programmable Peripheral products are supported with complete easy-to-use system development tools from both Data I/O and WSI. The Data I/O Unisite programmer can be used for production programming. The WSI tools include program development, simulation, and programming software, the IBM-PC hosted MagicPro™ Memory and Peripheral Programmer, a dial-in applications bulletin board and WSI's team of factory service and field application engineers. The menu-driven software tools run on popular customer owned computers and enable designers to rapidly configure and program the WSI part and try it in a prototype system. Additional design iterations are quickly accomodated. The system development tools increase the efficiency of the design process resulting in faster market entry for WSI's customers' products.

High-Performance Memory Products

WSI offers a broad product line of high-performance CMOS PROMs and EPROMs featuring architectures ranging from 2K x 8 to 512K x 8, with speeds ranging from 25 to 150 ns. Commercial, industrial and military products including MIL-STD-883C/SMD are available. A wide variety of package selections include plastic and hermetic, through-hole and surface mount types.

CMOS PROMs

As WSI's fastest family of products, Re-Programmable Read Only Memories (RPROMs) provide high-speed bipolar PROM pinout with matching speed and low power operation. The product family includes architectures ranging from 2K x 8 to 32K x 8 with speeds ranging from 25 to 70 ns. Commercial, industrial and military MIL-STD-883C/SMD configurations are available in a variety of hermetic and plastic package types.

"F" Family EPROMs

The high-speed "F" series EPROM family offers speeds ranging from 35 to 70 ns and architectures from 8K x 8 to 32K x 8. "F" family EPROMs are ideal for use in high-end engineering and scientific workstations, data communications and similar high-performance applications.

"L" Family Military EPROMs

WSI's "L" family military EPROM memory products feature high-density and high speed in popular JEDEC pinouts. With speeds ranging from 120 to 200 ns and architectures from 32K x 8 to 64K x 16, the "L" family offers significant speed and high density benefits for developers of military avionics, communications, and control systems. The "L" family delivers world class densities from WSI's conservative 1.2 micron lithography CMOS process technology.

Manufacturing

WSI's manufacturing strategy includes utilizing multiple world-class manufacturing partners for each facet of the production process.

WSI has licensed its CMOS EPROM and logic process technology to Sharp Corporation in Japan, National Semiconductor Corporation and Advanced Micro Devices (AMD), in the USA. The Sharp facility in Fukuyama, Japan employs the most advanced sub-micron VLSI integrated circuit manufacturing equipment available including ion implantation, reactive ion etch, and wafer stepper lithographic systems. The world-class high volume National Semiconductor operation delivers low cost production of 1.2 micron CMOS technology product on 6" wafers. This low defect density manufacturing resource is capable of producing sub-micron technology product in the near future. AMD produces a portion of WSI's programmable peripheral product requirements with a 1.2 micron process technology.

High-volume, low cost integrated circuit packaging and testing is performed for WSI by ANAM Electronics in Seoul, Korea, Fine Products in Hsinchu,Taiwan, National Semiconductor in Santa Clara, CA and at WSI in Fremont, CA. ANAM is the largest independent manufacturer of I.C. packaging and produces excellent product quality. Test capability ranges from simple logic devices to complex VLSI product. ANAM routinely processes a wide variety of high volume packages and enables WSI to leverage its materiel needs through ANAM's combined high-volume, low cost procurement activity. Commercial, industrial, and military grade product processing is available from ANAM.

Additional quality assurance and reliability testing are performed at WSI in Fremont, CA.

WSI's manufacturing strategy ensures the supply of multi-sourced high quality, high-volume product with competitive cost and fast delivery.

Sales Network

WSI's international sales network includes several regional sales managers who direct the resources of the company to major market opportunities. Experienced technical field application engineers located in each field office assist WSI's customers during their advanced product development and match customer needs with WSI's product solutions. Over sixty manufacturer's representatives and leading national and regional component distributors in the United States, Europe and Asia round out the WSI sales network.

United States

Direct sales and field application engineering offices in Boston, Chicago, Philadelphia, Dallas, Los Angeles and Fremont, CA; More than 25 manufacturer's representatives for major national accounts; national distributors include Arrow/Schweber, Time Electronics and Wyle Laboratories; and regional distributors.

International

Direct WSI Sales management offices in Paris, Munich and Hong Kong; sales representatives and distributors in Austria, Belgium, Denmark, England, Finland, France, Germany, Israel, Italy, Luxembourg, the Netherlands, Norway, Portugal, Spain, Sweden and Switzerland. Sales representatives and distributors for the Asia/Pacific Rim region in Australia, Hong Kong, India, Japan, Korea, Singapore and Taiwan.

Management and Previous Affiliations:

Michael Callahan
President, CEO and
Chairman of the Board
(Advanced Micro Devices, Monolithic Memories, Motorola)

Robert J. Barker
V. P. Finance, CFO and Secretary
(Monolithic Memories, Lockheed)

John Ekiss
V. P. Marketing
(Intel, Motorola)

Thomas Branch
V. P. Worldwide Sales
(Monolithic Memories, Fairchild)

George Kern
V. P. Operations
(Advanced Micro Devices, Monolithic Memories)

Boaz Eitan
V. P. New Product and
Technology Development
(Intel)

Bob Buschini
Director of Human Resources
(General Electric, Raychem)

Financing

WSI is a privately held California corporation founded in August, 1983. The company has been financed by corporate investors, institutional investors, venture capital groups and private investors. Corporate investors are Advanced Micro Devices, Sharp Corporation, National Semiconductor Corporation, Intergraph Corporation, and Kyocera Corporation. Venture capital investors include Accel Partners, Adler and Company, Bessemer Venture Partners, Genevest Consulting Group S. A.,J. H. Whitney, Oak Investment Partners, Robertson Stephens and Co., Smith Barney Venture Corporation, and Warburg Pincus. The company has been audited annually since its inception by Ernst & Young (Arthur Young prior to 1989) and regularly reports financial information to Dunn & Bradstreet (Dunns number is 10-209-8167).

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Product Selector Guide

July 1992

PROGRAMMABLE PERIPHERALS

SINGLE-CHIP CMOS USER-CONFIGURABLE PERIPHERALS WITH MEMORY – COMMERCIAL & MILITARY

Part No.	Description	EPROM	x8/x16	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection J	L	Q	X
PSD301	Programmable Microcontroller Peripherals with Memory; x8/x16;	256Kb	x8/x16	120		NOW	NOW	•	•	•	
				150-200		NOW	NOW	•	•	•	•
					200		NOW		•		•
PSD311	256Kb – 1Mb EPROM; 16K SRAM; PAD; System Features.	256Kb	x8	120		NOW	NOW	•	•	•	
				150-200		NOW	NOW	•	•	•	•
					200		NOW		•		•
PSD302		512Kb	x8/x16	120		NOW	NOW	•	•		
				150-200		NOW	NOW	•	•		
PSD312		512Kb	x8	120		NOW	NOW	•	•		
				150-200		NOW	NOW	•	•		
PSD303		1Mb	x8/x16	120		NOW	NOW	•	•		
				150-200		NOW	NOW	•	•		
PSD313		1Mb	x8	120		NOW	NOW	•	•		
				150-200		NOW	NOW	•	•		
PSD101	DSP Peripheral with Memory. Features: 128K Bits EPROM, 32K Bits SRAM, Programmable Address Decoder (PAD), Configurable: x8 or x16.			45-55		NOW	NOW	•	•	•	•
					55		NOW	•		•	

HIGH-PERFORMANCE CMOS PROGRAMMABLE PERIPHERAL CONTROLLER – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection Q	X	V
PAC1000	Programmable Peripheral Controller Optimized for High-Performance Control Systems. Key Features Include: 16-Bit CPU, 16-Bit Address Port, 16-Bit Output Control, 8-Bit I/O Port and Configuration Registers.	12MHz		NOW	NOW	•	•	•
			12MHz	NOW	NOW		•	•
		16MHz		NOW	NOW	•	•	

HIGH-PERFORMANCE CMOS USER-CONFIGURABLE MICROSEQUENCER/STATE MACHINE – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection J	L	S	T
SAM448	User-Programmable Microsequencer for Implementing High-Performance State Machines. Includes EPROM Integrated with Branch Control Logic, Pipeline Register, Stack and Loop Counter and 768 Product Terms.	20-25MHz		NOW	NOW	*	•	*	•
			20MHz	NOW	NOW				•

*J and S packages not available in 25MHz

SOFTWARE DEVELOPMENT TOOLS †

Part No.	Includes	Availability
PSD - GOLD	Contains PSD301/PSD101 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6014(J/L) or WS6015(X) Adapter and 2 Sample Devices.	NOW
PSD - SILVER	Contains PSD301/PSD101 Software and Users Manual	NOW
PAC1000 - GOLD	Contains PAC1000 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6010 (X) Adapter and 2 Sample Devices.	NOW
PAC1000 - SILVER	Contains PAC1000 Software and Users Manual	NOW
SAM448 - GOLD	Contains SAM448 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6008(T) or 6009(C,J,L) Adapter and 2 Sample Devices.	NOW
SAM448 - SILVER	Contains SAM448 Software and Users Manual	NOW
MEMORY - SILVER††	Contains WSI EPROM/RPROM Programming Software and Users Manual	NOW

† 1) All Development Systems include: 12 Month Software Update Service, access to WSI's 24 Hour Electronic Bulletin Board.
2) Package adaptor must be specified when ordering any "Gold" system.

†† 1) Memory-Silver is included in all development systems.

NON-VOLATILE MEMORY

CMOS PROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L	P	S	T
WS57C191B	2K x 8	16K CMOS PROM	35-55	•	•		•		
WS57C191C	2K x 8	16K CMOS PROM	25-55	•	•		•		
WS57C291B	2K x 8	16K CMOS PROM	35-55					•	•
WS57C291C	2K x 8	16K CMOS PROM	25-55					•	•
WS57C45	2K x 8	16K CMOS Reg. PROM	t_{SA} = 25-35					•	•
WS57C43B	4K x 8	32K CMOS PROM	35-70	•	•			•	•
WS57C43C	4K x 8	32K CMOS PROM	25-70	•	•			•	•
WS57C49B	8K x 8	64K CMOS PROM	35-70	•	•		•	•	•
WS57C49C	8K x 8	64K CMOS PROM	25-70	•	•			•	•
WS57C51C	16K x 8	128K CMOS PROM	35-70	•	•	•			•
WS57C71C	32K x 8	256K CMOS PROM	35*-70	•	•	•			•

*Consult closest WSI Sales Office for availability of 35 ns product.

CMOS PROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	F	H	K	T	Z
WS57C191B	2K x 8	16K CMOS PROM	45-55	•	•	•	•				•
WS57C291B	2K x 8	16K CMOS PROM	45-55	•					•	•	
WS57C45	2K x 8	16K CMOS Reg. PROM	35-45	•	•		•	•	•	•	•
WS57C43B	4K x 8	32K CMOS PROM	45-70		•	•	•			•	
WS57C43C	4K x 8	32K CMOS PROM	35-70		•	•	•			•	
WS57C49B	8K x 8	64K CMOS PROM	45-70	•	•	•	•			•	
WS57C49C	8K x 8	64K CMOS PROM	35-70	•	•	•	•			•	
WS57C51C	16K x 8	128K CMOS PROM	45-55		•	•				•	
WS57C71C	32K x 8	256K CMOS PROM	55-70		•	•				•	

NON-VOLATILE MEMORY (Cont.)

HIGH-SPEED CMOS EPROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L	P	T
WS57C64F	8K x 8	High-Speed 64K CMOS EPROM	55-70	•	•			
WS57C128F	16K x 8	High-Speed 128K CMOS EPROM	55-70	•				
WS57C128FB	16K x 8	High-Speed 128K CMOS EPROM	35-45	•	•	•		
WS57C256F	32K x 8	High-Speed 256K CMOS EPROM	45-70	•	•	•	•	•

HIGH-SPEED CMOS EPROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	T	L
WS57C64F	8K x 8	High-Speed 64K CMOS EPROM	70	•	•	•		
WS27C64F	8K x 8	Low-Power 64K CMOS EPROM	90	•	•	•		
WS57C128F	16K x 8	High-Speed 128K CMOS EPROM	70	•	•	•		
WS57C128FB	16K x 8	High-Speed 128K CMOS EPROM	45-55		•	•		
WS27C128F	16K x 8	Low-Power 128K CMOS EPROM	90	•	•	•		
WS57C256F	32K x 8	High-Speed 256K CMOS EPROM	55-70	•	•	•	•	
WS27C256F	32K x 8	Low-Power 256K CMOS EPROM	90	•	•	•	•	

CMOS BIT SLICE AND LOGIC

Part No.	Description	Speed		Package Selection							
		Comm'l	Military	B	G	J	K	L	P	S	Y
WS5901	4-Bit CMOS Bit Slice Processor	32,43 MHz	32,43MHz						•		•
WS59016	16-Bit CMOS Bit Slice Processor	15 MHz	12.5MHz	•		•		•			
WS59032	32-Bit CMOS Bit Slice Processor	26.4,33 MHz	23.6,29 MHz		•						
WS5910	CMOS Microprogram Controller	20,30 MHz	20,30 MHz						•		•
WS59510	16K x 16 CMOS Multiplier-Accum.	30-50 ns			•	•			•		
WS59520	CMOS Pipeline Register	Tpd = 22ns	Tpd = 24ns				•			•	
WS59521	CMOS Pipeline Register	Tpd = 22ns	Tpd = 24ns				•			•	
WS59820	CMOS Bi-Directional Register	Tpd = 23ns	Tpd = 25ns		•	•					

WSI PACKAGE DESCRIPTIONS

Package Code	Description	Window	Surface Mount	Plastic/OTP
B/R	Ceramic Sidebrazed Dip	N/Y	N	–
C	Ceramic Leadess Chip Carrier (CLLCC)	Y	Y	–
C/Z	Ceramic Leadless Chip Carrier (CLLCC)	Y/N	Y	–
D/Y	0.600" Ceramic Dip	Y/N	N	–
F/H	Ceramic Flatpack	Y/N	Y	–
J	Plastic Leaded Chip Carrier (PLDCC)	N	Y	Y
L/N	Ceramic Leaded Chip Carrier (CLDCC)	Y/N	Y	–
P	Plastic Dip	N	N	Y
Q	Plastic Quad Flatpack (PQFP)	N	Y	Y
S	0.300" Plastic Dip	N	N	Y
T/K	0.300" Ceramic Dip	Y/N	N	–
V	Ceramic Quad Flatpack (CQFP)	Y	Y	–
X/G	Ceramic Pin Grid Array (CPGA)	Y/N	N	–

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USA Southwest:	Tel: 714-753-1180	Fax: 714-753-1179
USA Midwest:	Tel: 708-882-1893	Fax: 708-882-1881
USA Southeast:	Tel: 214-680-0077	Fax: 214-680-0280
USA Mid-Atlantic:	Tel: 215-638-9617	Fax: 215-638-7326
USA Northeast:	Tel: 508-685-6101	Fax: 508-685-6105
Europe (France):	Tel: 33 (1) 69-32-01-20	Fax: 33 (1) 69-32-02-19
Europe (Germany)	Tel: (49) 89.23.11.38.49	Fax: (49) 89.23.11.38.11
Asia (Hong Kong)	Tel: 852-575-0112	Fax: 852-893-0678

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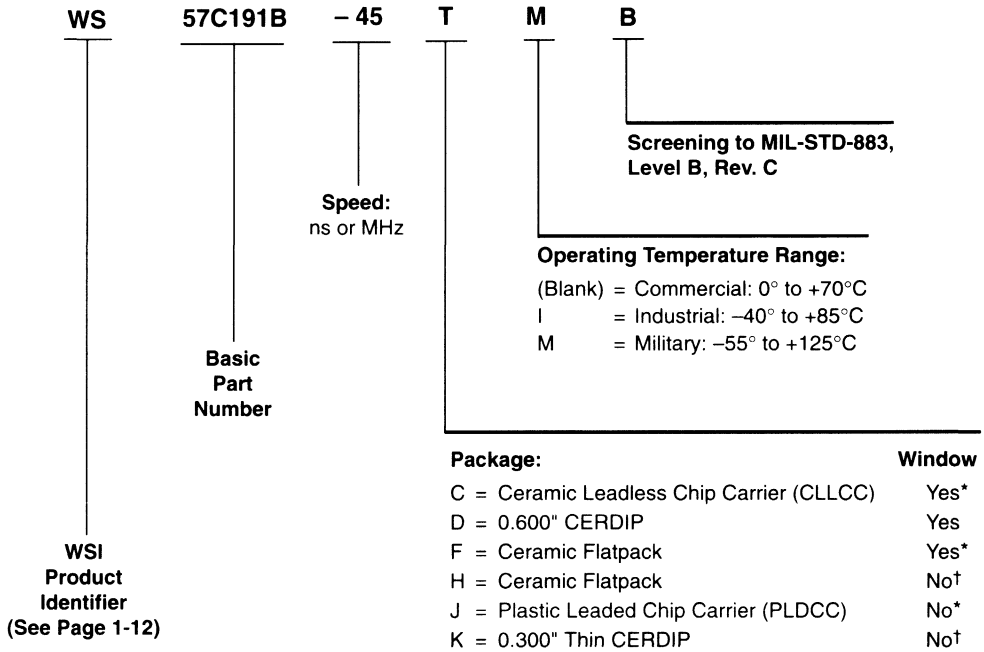
Ordering Information
High-Performance CMOS Memory Products

Part Number Explanation:



Package:	Window
C = Ceramic Leadless Chip Carrier (CLLCC)	Yes*
D = 0.600" CERDIP	Yes
F = Ceramic Flatpack	Yes*
H = Ceramic Flatpack	No†
J = Plastic Leaded Chip Carrier (PLDCC)	No*
K = 0.300" Thin CERDIP	No†
L = Ceramic Leaded Chip Carrier (CLDCC)	Yes**
P = 0.600" Plastic DIP	No
S = 0.300" Thin Plastic DIP	No
T = 0.300" Thin CERDIP	Yes
W = Waffle Packed Dice	–
Y = 0.600" CERDIP	No
Z = Ceramic Leadless Chip Carrier (CLLCC)	No†

*Surface Mount.
**Socketing Recommended.
†Non-Windowed Ceramic Packages for Mil Products Only.

WSI Product Marking

- For all WSI Product the "WS" portion of the part number **IS NOT** included in the actual part marking on the device package. For example, the WSI product WS57C291B-35T will be observed as 57C291B-35T on the package marking.
- The standard marking always includes:

  The WSI Logo, the Part Number, and the Data Code.
- All WSI products currently carry a back marking which consists of:
  - The assembly country of origin.
  - A lot code identifier.
  - The part number without a speed or package suffix.

  (This back marking is subject to change at WSI's discretion and without notice.)
- SMD products will always carry the following markings:
  - The WSI Logo, the Date Code, an ESD Designator ( ), and the SMD Number.

  WSI's 600 mil DIP SMD packages will also carry the WSI part number as well as the SMD marking. This is for the convenience of WSI and its distributors only, and is not required or excluded by the Mil Spec, or the SMD drawing. This dual marking is not possible with all product configurations due to the space limitations of several of the smaller packages, in particular those with windows.

Advance Information/ Preliminary/Final Defined

Advance Information

A WSI product data sheet marked "Advance Information" on its cover page describes a product that is in the planning stages at WSI at the time this book went to press and is planned to sample in the current year. Please contact your WSI Sales Representative or Distributor for availability status.

Preliminary

A WSI product data sheet marked "Preliminary" on its cover page describes a product that is in early production and is subject to additional characterization testing. Functionality is finalized but electrical limits may be subject to change before the data sheet is "Final." Please contact your WSI Sales Representative or Distributor for price and availability.

Final

A WSI product data sheet without either "Advance Information" or "Preliminary" on the cover page describes a product that has completed all characterization and reliability testing. All functional and electrical parameters are believed to be accurate and reliable. Please contact your WSI Sales Representative or Distributor for price and availability.

Section Index

PROM//RPROM Memory Products

For additional information, call 800-TEAM-WSI (800-832-6974). In California, Call 800-562-6363.

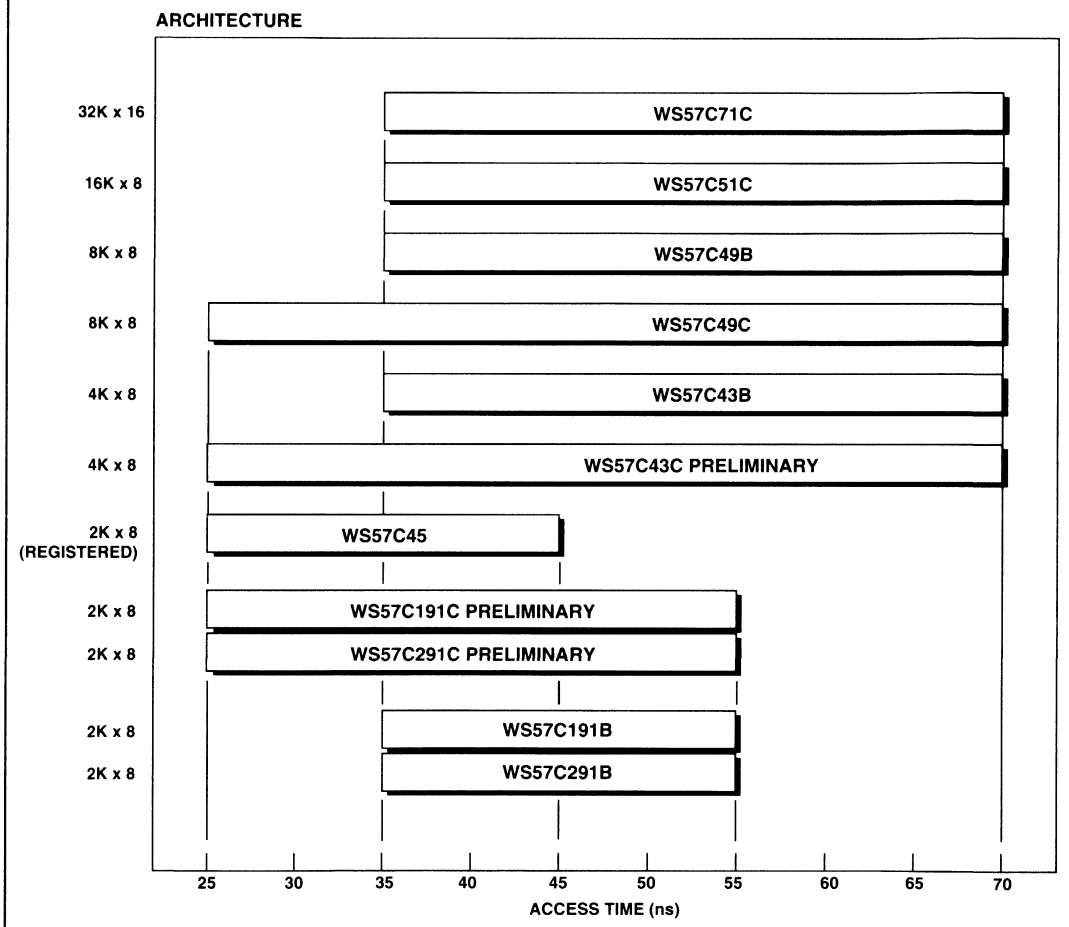
FAMILY OF HIGH PERFORMANCE CMOS PROMs AND RPROMs

PART NUMBER	PAGE NO.	DENSITY (BITS)	ARCHITECTURE	SPEED (NS)	DRAWING NO.	NO. OF PINS	PACKAGE
WS57C191B	2-7	16K	2K x 8	35 – 55	C1	28	CLLCC
					D1	24	CERDIP, 0.6"
					F1	24	Ceramic Flatpack
					J3	28	PLDCC
					P2	24	Plastic DIP, 0.6"
					Y3	24	CERDIP, 0.6"
					Z2	28	CLLCC
WS57C191C	2-13	16K	2K x 8	25 – 55	D1	24	CERDIP, 0.6"
					J3	28	PLDCC
					P2	24	Plastic DIP, 0.6"
WS57C291B	2-7	16K	2K x 8	35 – 55	K1	24	CERDIP, 0.3"
					S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"
WS57C291C	2-13	16K	2K x 8	25 – 55	S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"
WS57C45 (Registered)	2-19	16K	2K x 8	25 – 45	C1	28	CLLCC
					F1	24	Ceramic Flatpack
					H1	24	Ceramic Flatpack
					K1	24	CERDIP, 0.3"
					S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"
WS57C43B	2-27	32K	4K x 8	35 – 70	C1	28	CLLCC
					D1	24	CERDIP, 0.6"
					J3	28	PLDCC
					S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"
					Y3	24	CERDIP, 0.3"
WS57C43C	2-33	32K	4K x 8	25 – 70	D1	24	CERDIP, 0.6"
					J3	28	PLDCC
					S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"
					Y3	24	CERDIP, 0.3"
WS57C49B	2-39	64K	8K x 8	35 – 70	C1	28	CLLCC
					D1	24	CERDIP, 0.6"
					F1	24	Ceramic Flatpack
					J3	28	PLDCC
					S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"

FAMILY OF HIGH PERFORMANCE CMOS PROMs AND RPROMs (Cont.)

PART NUMBER	PAGE NO.	DENSITY (BITS)	ARCHITECTURE	SPEED (NS)	DRAWING NO.	NO. OF PINS	PACKAGE
WS57C49C	2-45	64K	8K x 8	25 – 70	C1	28	CLLCC
					D1	24	CERDIP, 0.6"
					F1	24	Ceramic Flatpack
					J3	28	PLDCC
					L2	28	CLDCC
					S1	24	Plastic DIP, 0.3"
					T1	24	CERDIP, 0.3"
WS57C51C	2-51	128K	16K x 8	35 – 70	C2	32	CLLCC
					D2	28	CERDIP, 0.6"
					J4	32	PLDCC
					L3	32	CLDCC
					T2	28	CERDIP, 0.3"
WS57C71C	2-57	256K	32K x 8	35 – 70	C2	32	CLLCC
					D2	28	CERDIP, 0.6"
					J4	32	PLDCC
					L3	32	CLDCC
					T2	28	CERDIP, 0.3"

WSI's Family of High Performance CMOS PROMs and RPROMs (Re-Programmable Read Only Memory) are available in all three operating temperature ranges: Commercial (0 to +70°C), Industrial (–40 to +85°C) and Military (–55 to +125°C). In addition, several versions are available as Standard Military Drawing (SMD) products.


ARCHITECTURE
32K x 16
16K x 8
8K x 8
8K x 8
4K x 8
4K x 8
2K x 8
(REGISTERED)
2K x 8
2K x 8
2K x 8
2K x 8
WS57C71C
WS57C51C
WS57C49B
WS57C49C
WS57C43B
WS57C43C PRELIMINARY
WS57C45
WS57C191C PRELIMINARY
WS57C291C PRELIMINARY
WS57C191B
WS57C291B
25
30
35
40
45
50
55
60
65
70
ACCESS TIME (ns)

AMD	WSI
AM27C49	WS57C49B/49C
AM27C191	WS57C291B
AM27C291	WS57C291B
AM27PS43	WS57C43B/43C
AM27S43	WS57C43B/43C
AM27S43A	WS57C43B/43C
AM27S45	WS57C45
AM27S49	WS57C49B/49C
AM27S51	WS57C51C
AM27S51A	WS57C51C
AM27S191	WS57C191B
AM27S291	WS57C291B

ATMEL	WSI
AT27HC641R/2	WS57C49/49B/49C

CYPRESS	WSI
CY7C245	WS57C45
CY7C245A	WS57C45
CY7C251	WS57C51C
CY7C253	WS57C51C
CY7C254	WS57C51C
CY7C261	WS57C49B/49C
CY7C263	WS57C49B/49C
CY7C264	WS57C49B/49C
CY7C271	WS57C71C
CY7C291	WS57C291/B
CY7C292	WS57C191/B

FUJITSU	WSI
MBH38H	WS57C191B
MBH38-SK	WS57C291B
MB7142	WS57C43B/43C
MB7143	WS57C49B/49C
MB7144E	WS57C49B/49C
MB7144H	WS57C49B/49C

HITACHI	WSI
HN25169	WS57C191B
HN25169	WS57C291B

ICT	WSI
27CX321	WS57C43B/43C
27CX322	WS57C43B/43C
27CX641	WS57C49B/49C
27CX642	WS57C49B/49C

MOTOROLA	WSI
MCM76	WS57C191B
MCM76160	WS57C291B
MCM76161	WS57C291B

NATIONAL	WSI
87S321	WS57C43B/43C
93Z665C	WS57C49B/49C
93Z667C	WS57C49B/49C
DM77S321	WS57C43B/43C
DM87S291	WS57C291B
DM87S291A	WS57C291B
DM87S291B	WS57C291B
DM87S321	WS57C43B/43C
DM87SR191	WS57C191B
DM87SR193	WS57C191B

NEC	WSI
27HC65	WS57C49B/49C
µPB 429	WS57C191B
µPB 429	WS57C291B

SHARP	WSI
LH5749	WS57C49B/49C
LH57127	WS57C51C
LH57191	WS57C191/B
SH5762	WS57C49B/49C

SIGNETICS	WSI
27HC641	WS57C49B/49C
27HC642	WS57C49B/49C
N82HS321	WS57C43B/43C
N82HS641	WS57C49B/49C
N82HS1281	WS57C51C
N82S191	WS57C191B
N82S191	WS57C291B
N82S191A	WS57C191B
N82S191A	WS57C291B
N82S191B	WS57C191B
N82S191B	WS57C291B
N82S641	WS57C49B/49C

SSI	WSI
SS1203	WS57C49B/49C

THOMSON	WSI
JBP38S165	WS57C191B
JBP38S165	WS57C291B

TI	WSI
38S165	WS57C191B
38S165	WS57C291B
TMS27C291	WS57C191B
TMS27C292	WS57C291B
TMS27PC49	WS57C49B/49C

HIGH SPEED 2K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD Nos. 5962-87650/5962-88734**
- **Pin Compatible with Am27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000 V**

2

GENERAL DESCRIPTION

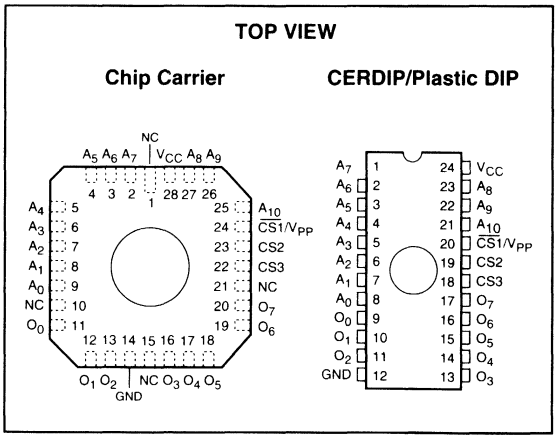
The WS57C191B/291B is an extremely High Performance 16K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. The WS57C191B/291B is also configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

The WS57C191B is packaged in a conventional 600 mil DIP package as well as a leadless chip carrier.The WS57C291B is packaged in a space saving 300 mil DIP package configuration. Both are available in commercial, industrial, and military operating temperature ranges.

MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IL}	V_{CC}	High Z

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	191B/291B-35	191B/291B-45	191B/291B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
CS to Output Valid Time (Max)	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with
Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

ESD Protection .....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Industrial		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

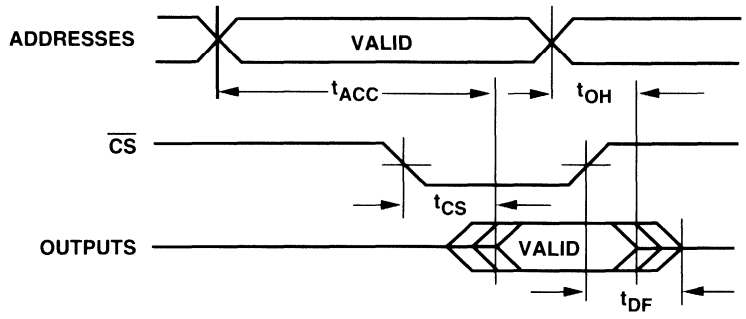
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	191B/291B-35		191B/291B-45		191B/291B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20	
Output Disable to Output Float*	t_{DF}		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

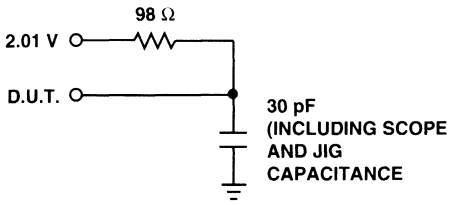


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

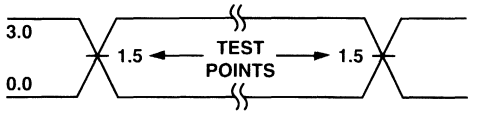
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

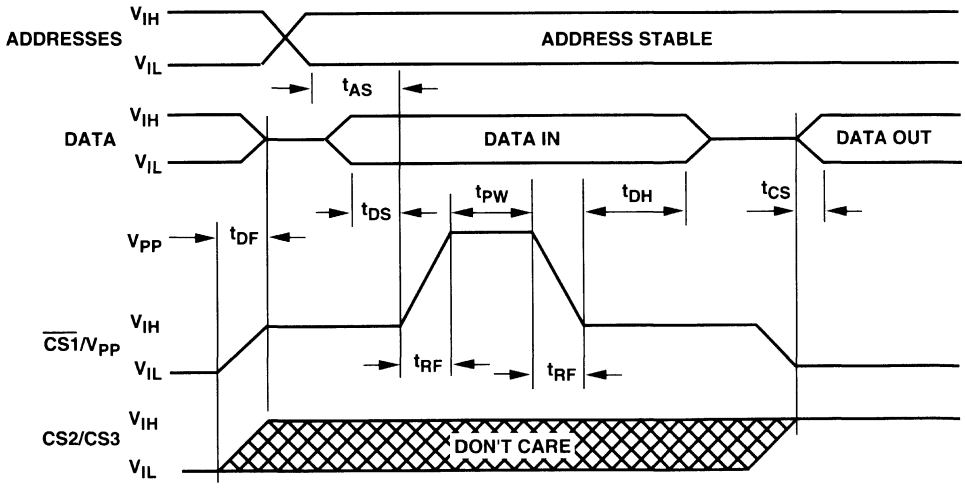
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4 mA)	2.4		V

NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191B					
WS57C191B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-45CMB*	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C191B-45DMB*	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-45FMB*	45	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C191B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-45YMB*	45	24 Pin CERDIP, 0.6"	Y3	Military	MIL-STD-883C
WS57C191B-45ZMB*	45	28 Pad CLLCC	Z2	Military	MIL-STD-883C
WS57C191B-50CMB*	50	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-50DMB*	50	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-55DMB*	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-55ZMB*	55	28 Pad CLLCC	Z2	Military	MIL-STD-883C
WS57C291B					
WS57C291B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-45KMB*	45	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C291B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C291B-45TMB*	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291B-50TMB*	50	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291B-55KMB*	55	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C291B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-55TMB*	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: 9. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C191B and WS57C291B are programmed using Algorithm A shown on page 5-3.

HIGH SPEED 2K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — t_{ACC} = 25 ns
  - — t_{CS} = 12 ns
- **Low Power Consumption**
- **Fast Programming**
- **Available in 300 Mil DIP and PLDCC**
- **Pin Compatible with Am27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**

2

GENERAL DESCRIPTION

The WS57C191C/291C is an extremely High Performance 16K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. The WS57C191C/291C is also configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

The WS57C191C is packaged in a conventional 600 mil DIP package as well as a Plastic Leaded Chip Carrier (PLDCC) and a Ceramic Leadless Chip Carrier (CLLCC). The WS57C291C is packaged in a space saving 300 mil DIP package configuration. Both are available in commercial, industrial, and military operating temperature ranges.

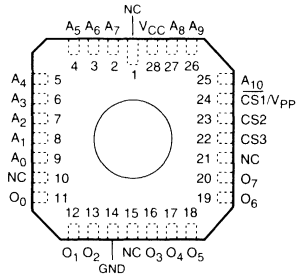
MODE SELECTION

MODE \ PINS	$\overline{CS1}$/V_{PP}	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IL}	V_{CC}	High Z

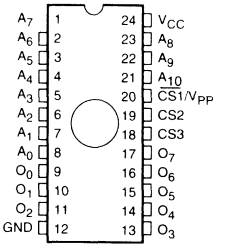
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	191C/291C-25	191C/291C-35	191C/291C-45	191C/291C-55
Address Access Time (Max)	25 ns	35 ns	45 ns	55 ns
CS to Output Valid Time (Max)	12 ns	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Industrial		50	mA
			Military		50	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

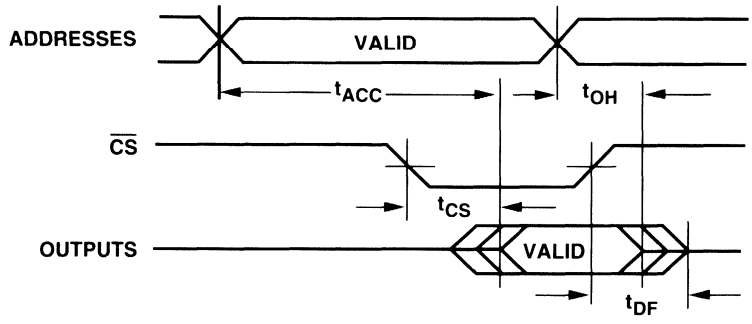
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	191C/291C-25		191C/291C-35		191C/291C-45		191C/291C-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		25		35		45		55	ns
$\overline{CS}$ to Output Delay	t_{CS}		12		20		20		20	
Output Disable to Output Float*	t_{DF}		12		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

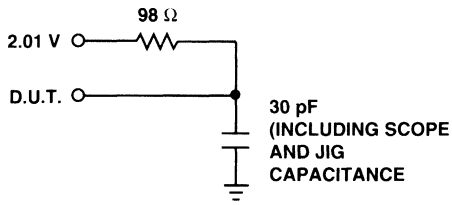


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

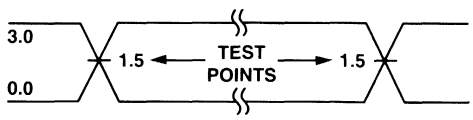
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for TA = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

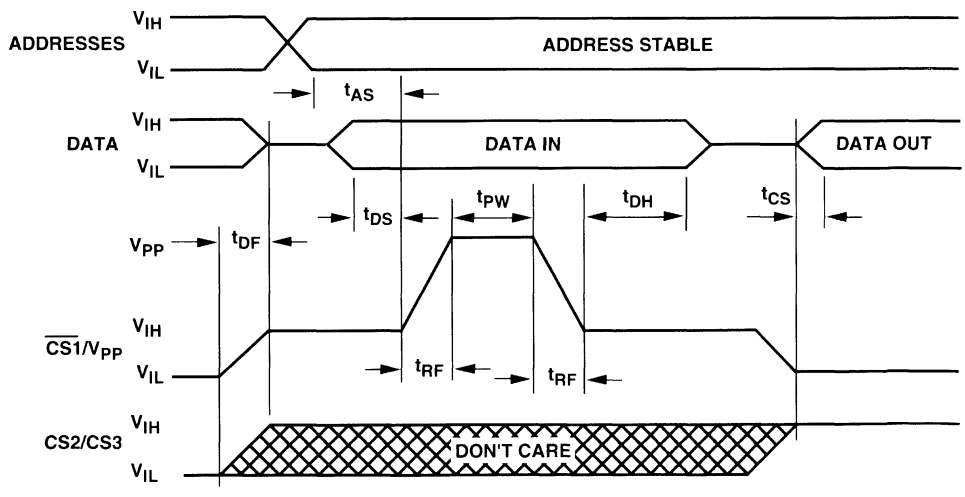
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4 mA)	2.4		V

NOTES: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191C					
WS57C191C-25D	25	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-25J	25	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191C-25P	25	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191C-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191C-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191C-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C191C-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191C-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191C-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191C-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C291C					
WS57C291C-25S	25	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291C-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291C-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291C-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C291C-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291C-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: 9. The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C191C and WS57C291C are programmed using Algorithm D shown on page 5-7.

HIGH-SPEED 2K x 8 REGISTERED CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 25 ns Setup
  - — 12 ns Clock to Output
- **Low Power Consumption**
- **Fast Programming**
- **Programmable Synchronous or Asynchronous Output Enable**
- **DESC SMD Nos. 5962-88735/5962-87529**
- **Pin Compatible with AM27S45 and CY7C245**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Programmable Asynchronous Initialize Register**

2

GENERAL DESCRIPTION

The WS57C45 is an extremely HIGH PERFORMANCE 16K UV Erasable Registered CMOS RPROM. It is a direct drop-in replacement for such devices as the AM27S45 and CY7C245.

To meet the requirements of systems which execute and fetch instructions simultaneously, an 8-bit parallel data register has been provided at the output which allows RPROM data to be stored while other data is being addressed.

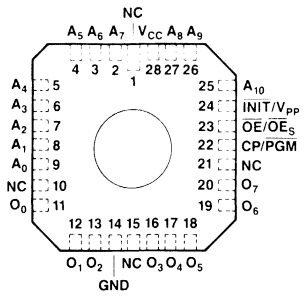
An asynchronous initialization feature has been provided which enables a user programmable 2049th word to be placed on the outputs independent of the system clock. This feature can be used to force an initialize word or provide a preset or clear function.

A further advantage of the WS57C45 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C45 RPROM in a windowed package is 100% tested with worst case test patterns both before and after assembly.

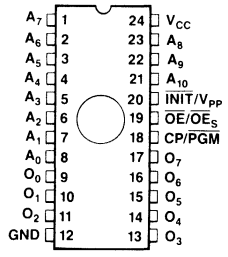
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP/ Flatpack



PRODUCT SELECTION GUIDE

PARAMETER	WS57C45-25	WS57C45-35	WS57C45-45
Set Up Time (Max)	25 ns	35 ns	45 ns
Clock to Output (Max)	12 ns	15 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....−65° to + 150°C

Voltage on any Pin with Respect to Ground .....−0.6V to +7V

V_{PP} with Respect to Ground.....−0.6V to + 14V

ESD Protection .....>2000V

*NOTICE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)	Comm'l		20	mA
			Industrial		30	mA
			Military		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)	Comm'l		25	mA
			Industrial		35	mA
			Military		35	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 2 mA/MHz for A.C. power component.
4. This parameter is only sampled and is not 100% tested.

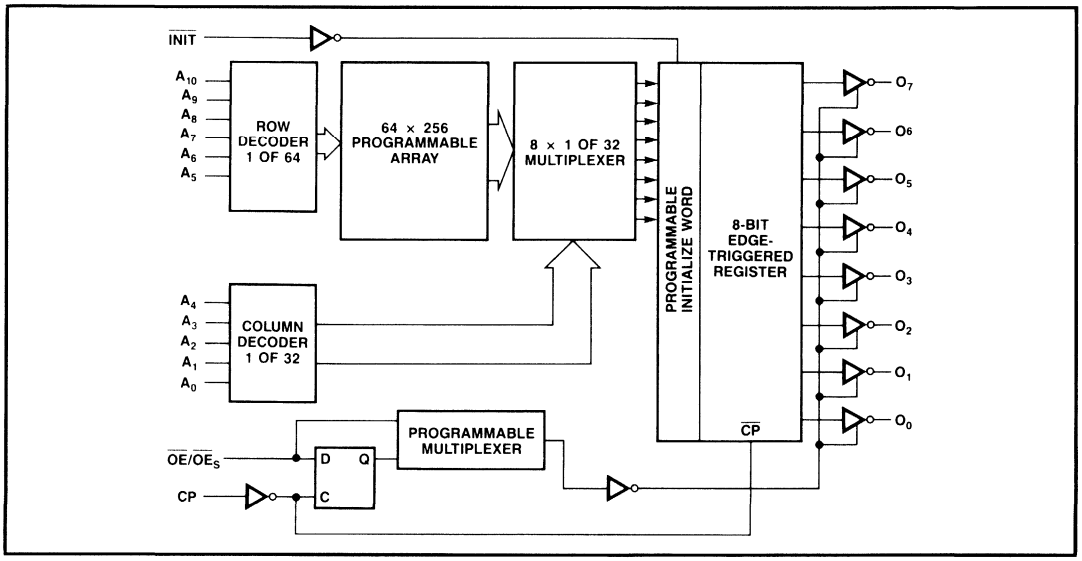
CAPACITANCE(4)

SYMBOL	PARAMETER	CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V	5	pF
C_{OUT}	Output Capacitance		8	pF

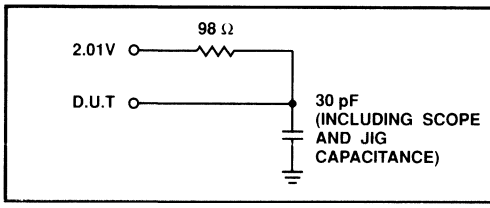
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C45-25		WS57C45-35		WS57C45-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Setup to Clock High	t_{SA}	25		35		45		ns
Address Hold From Clock High	t_{HA}	0		0		0		ns
Clock High to Valid Output	t_{CO}		12		15		25	ns
Clock Pulse Width	t_{PWC}	15		20		20		ns
$\overline{OE}_S$ Setup to Clock High	t_{SOE_S}	12		15		15		ns
$\overline{OE}_S$ Hold From Clock High	t_{HOE_S}	5		5		5		ns
Delay From INIT to Valid Output	t_{DI}		20		20		35	ns
$\overline{INIT}$ Recovery to Clock High	t_{RI}	15		20		20		ns
$\overline{INIT}$ Pulse Width	t_{PWI}	15		20		25		ns
Active Output From Clock High	t_{LZC}		15		20		30	ns
Inactive Output From Clock High	t_{HZC}		15		20		30	ns
Active Output From $\overline{OE}$ Low	t_{LZOE}		15		20		30	ns
Inactive Output From $\overline{OE}$ High	t_{HZOE}		15		20		30	ns

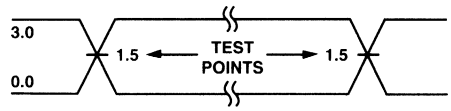
BLOCK DIAGRAM



TEST LOAD (High Impedance Test Systems)

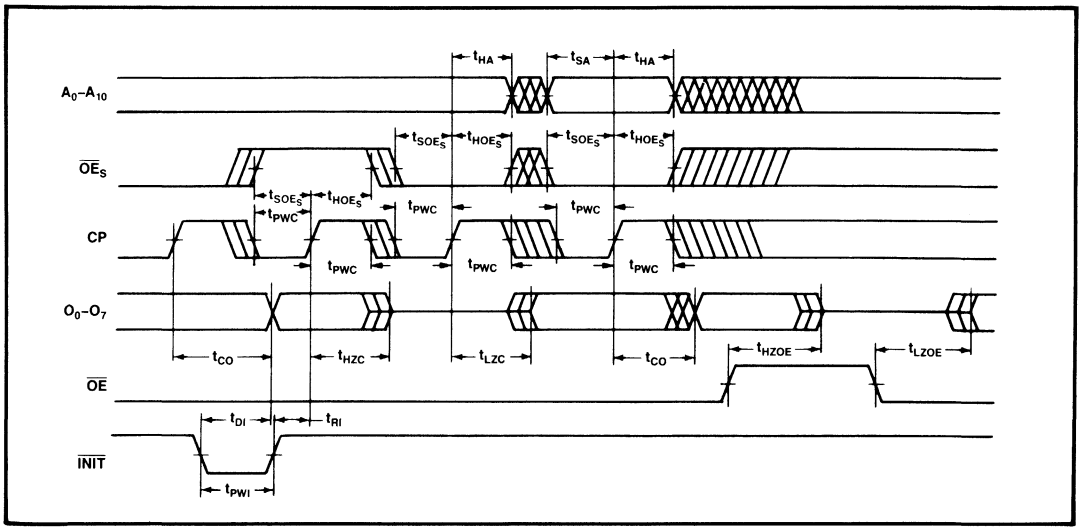


A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

AC READ TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The WS57C45 is an electrically programmable read only memory produced with WSI's patented high-performance self-aligned split-gate CMOS EPROM technology. It is organized as 2048 × 8 bits and is pin-for-pin compatible with bipolar TTL fuse link PROMs. The WS57C45 includes a D-type 8-bit data register on-chip which reduces the complexity and cost of microprogrammed pipelined systems where PROM data is held temporarily in a register. The circuit features a programmable synchronous ($\overline{OE_S}$) or asynchronous ($\overline{OE}$) output enable and asynchronous initialization ($\overline{INIT}$).

The programmed state of the enable pin ($\overline{OE_S}$ or $\overline{OE}$) will dictate the state of the outputs at power up. If $\overline{OE_S}$ has been programmed, the outputs will be in the OFF or high impedance state. If $\overline{OE}$ has been programmed, the outputs will be OFF or high impedance only if the $\overline{OE}$ input is HIGH. Data is read by applying the address to inputs A_{10}–A_0 and a LOW to the enable input. The data is retrieved and loaded into the master section of the 8-bit data register during the address set-up time. The data is transferred to the slave output of the data register at the next LOW to HIGH clock (CP) transition. Then the output buffers present the data on the outputs (0_7–0_0).

When using the asynchronous enable ($\overline{OE}$), the output buffers may be disabled at any time by switching the enable input to a logic HIGH. They may be re-enabled by switching the enable to a logic LOW.

When using the synchronous enable ($\overline{OE_S}$), the outputs revert to a high impedance or OFF state at the next positive clock edge following the $\overline{OE_S}$ input transition to a HIGH state. The output will revert to the active state following a positive clock edge when the $\overline{OE_S}$ input is at a LOW state. The address and synchronous enable inputs are free to change following a positive clock edge since the output will not change until the next low to high clock transition. This enables accessing the next data location while previously addressed data is present on the outputs.

To avoid race conditions and simplify system timing, the 8-bit edge triggered data register clock is derived directly from the system clock.

The WS57C45 has an asynchronous initialize input ($\overline{INIT}$). This function can be used during power-up and time-out periods to implement functions such as a start address or initialized bus control word. The $\overline{INIT}$ input enables the contents of a 2049th 8-bit word to be loaded directly into the output data register. The $\overline{INIT}$ input can be used to load any 8-bit data pattern into the register since each bit is programmable by the user. When unprogrammed, activating $\overline{INIT}$ will result in clearing the register (outputs LOW). When all bits are programmed, activating $\overline{INIT}$ results in PRESETting the register (outputs HIGH).

When activated LOW, the $\overline{INIT}$ input results in an immediate load of the 2049th word into both the master and slave sections of the output register. This is independent of any other input including the clock (CP) input. The initialize data will be present at the outputs after the asynchronous enable ($\overline{OE}$) is taken to a LOW state.

Programming Information

Apply power to the WS57C45 for normal read mode operation with CP/$\overline{PGM}$, $\overline{OE}$/$\overline{OE_S}$ and $\overline{INIT}$/V_{PP} at V_{IH}. Then take $\overline{INIT}$/V_{PP} to V_{PP}. The part is then in the program inhibit mode operation and the output lines are in a high impedance state. Refer to figure 5. As shown in figure 5, address, program and verify one byte of data. Repeat this sequence for each location to be programmed.

When intelligent programming is used, the program pulse width is 1 ms in length. Each address location is programmed and verified until it verifies correctly up to and including 5 times. After the location verifies, an additional programming pulse should be applied that is X1 times in duration of the sum of the previous programming pulses before proceeding on to the next address and repeating the process.

Initialization Byte Programming

The WS57C45 has a 2049th byte of data that can be used to initialize the value of the data register. This byte contains the value "0" when it is shipped from the factory. The user must program the 2049th byte with a value other than "0" for data register initialization if that value is not desired. Except for the following details, the user may program the 2049th byte in the same manner as the other 2048 bytes. First, since all 2048 addresses are used up, a super voltage address feature is used to enable an additional address. The actual address includes V_{PP} on A_1 and V_{IL} on A_2. Refer to the Mode Selection table. The programming and verification of the Initial Byte is accomplished operationally by performing an initialize function.

Synchronous Enable Programming

The WS57C45 contains both a synchronous and asynchronous enable feature. The part is delivered configured in the asynchronous mode and only requires alteration if the synchronous mode is required. This is accomplished by programming an on-chip EPROM cell. Similar to the Initial Byte, this function is enabled and addressed by using a super voltage. Referring to the Mode Selection table, V_{PP} is applied to A_1 followed by V_{IH} applied to A_2. This procedure addresses the EPROM cell that programs the synchronous enable feature. The EPROM cell is programmed with a 10 ms program pulse on CP/$\overline{PGM}$. It does not require any data since there is no selection as to how synchronous enable may be programmed, only if it is to be programmed.

Synchronous Enable Verification

The WS57C45's synchronous enable function is verified operationally. Apply power for read operation with $\overline{OE}/\overline{OE_S}$ and $\overline{INIT}/V_{PP}$ at V_{IH} and take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH}. The output data bus should be in a high impedance state. Next take $\overline{OE}/\overline{OE_S}$ to V_{IL}. The outputs will remain in the high impedance state. Take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH} and the outputs will now contain the data that is present. Take $\overline{OE}/\overline{OE_S}$ to V_{IH}. The output should remain driven. Clocking CP/$\overline{PGM}$ once more from V_{IL} to V_{IH} should place the outputs again in a high impedance state.

2

Blank Check

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C45 has all 2048 bytes in the '0' state. "1's" are loaded into the WS57C45 through the procedure of programming.

MODE SELECTION

MODE	READ OR OUTPUT DISABLE	PIN FUNCTION					OUTPUTS
		A_2	CP/$\overline{PGM}$	($\overline{OE}/\overline{OE_S}$)/$\overline{VFY}$	$\overline{INIT}/V_{PP}$	A_1	
Read[6]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable		X	X	V_{IH}	V_{IH}	X	High Z
Program[5,7]		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Verify[5,7]		X	V_{IH}	V_{IL}	V_{PP}	X	Data Out
Program Inhibit[5,7]		X	V_{IH}	V_{IH}	V_{PP}	X	High Z
Intelligent Program[5,7]		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Synch Enable[7]		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	High Z
Program Initial Byte[7]		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	Data In
Initial Byte Read		X	X	V_{IL}	V_{IL}	X	Data Out

NOTES:

5. X = Don't care but not to exceed V_{PP}.
6. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
7. During programming and verification, all unspecified pins to be at V_{IL}.

FIGURE 5. PROM PROGRAMMING WAVEFORMS

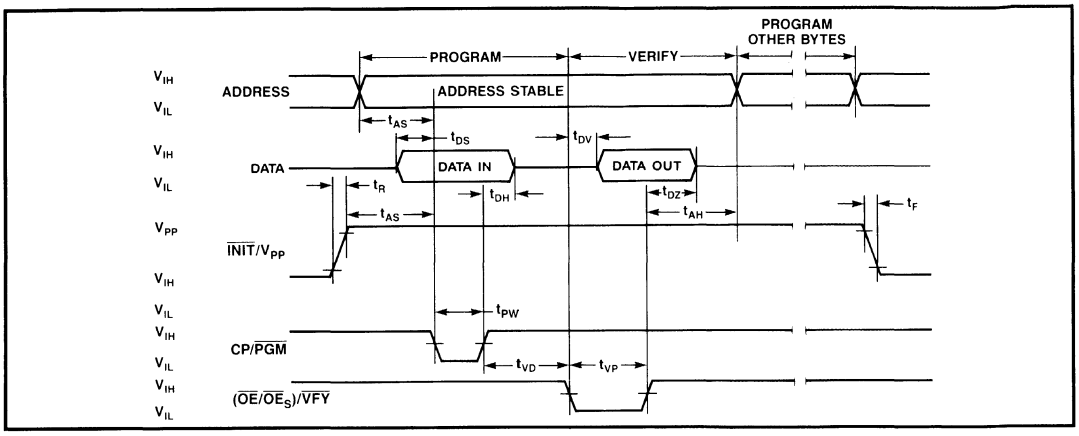


FIGURE 6. INITIAL BYTE PROGRAMMING WAVEFORMS

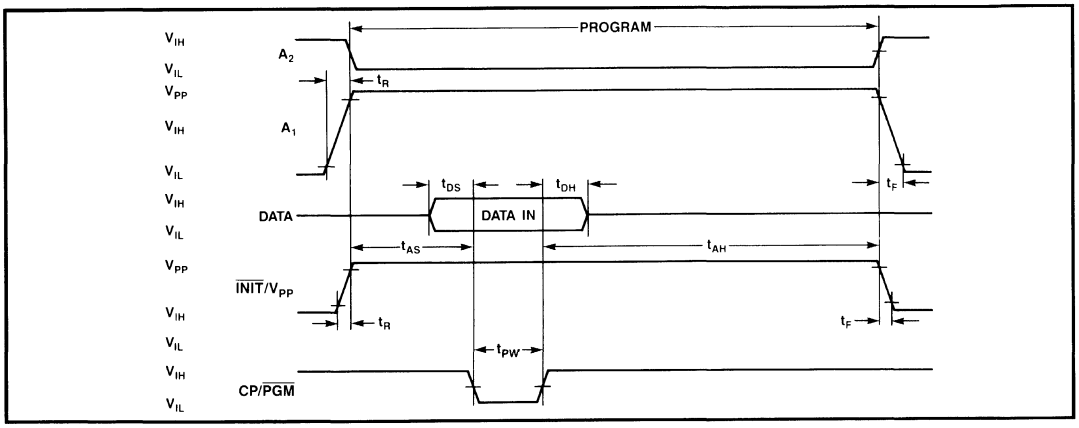
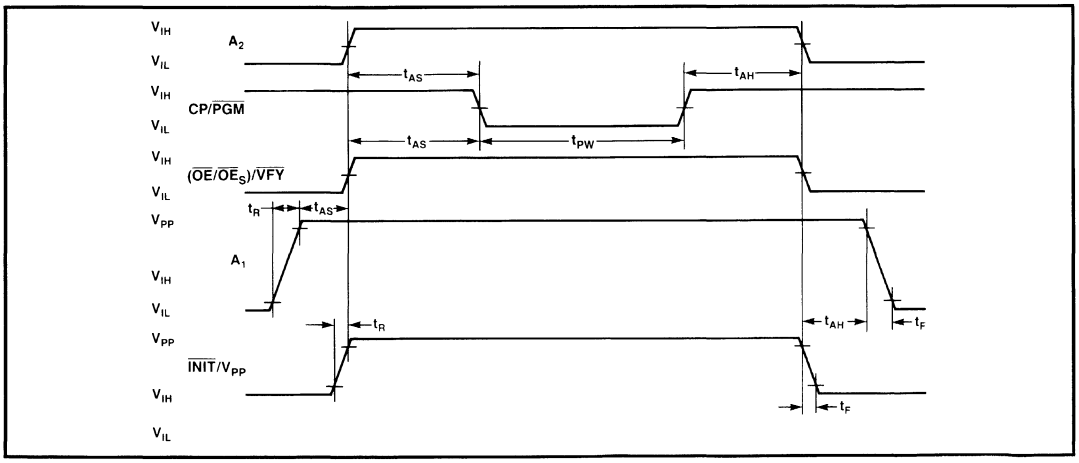


FIGURE 7. PROGRAM SYNCHRONOUS ENABLE



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Voltage	V_{IL}	−0.1	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{PW}	Programming Pulse Width	0.1	10	ms
t_{AS}	Address Setup Time	1.0		µs
t_{DS}	Data Setup Time	1.0		µs
t_{AH}	Address Hold Time	1.0		µs
t_{DH}	Data Hold Time	1.0		µs
t_R, t_F	V_{PP} Rise and Fall Time	1.0		µs
t_{VD}	Delay to $\overline{VFY}$	1.0		µs
t_{VP}	$\overline{VFY}$ Pulse Width	2.0		µs
t_{DV}	$\overline{VFY}$ Data Valid		1.0	µs
t_{DZ}	$\overline{VFY}$ HIGH to High Z		1.0	µs

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C45-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35CMB*	35	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C45-35HMB*	35	24 Pin Ceramic Flatpack	H1	Military	MIL-STD-883C
WS57C45-35KMB*	35	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C45-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C45-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35TMB*	35	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C45-45CMB*	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C45-45FMB*	45	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C45-45HMB*	45	24 Pin Ceramic Flatpack	H1	Military	MIL-STD-883C
WS57C45-45KMB*	45	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C45-45T	45	28 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-45TMB*	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD numbers.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C45 is programmed using Algorithm A shown on page 5-3.

HIGH SPEED 4K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with Am27S43 and N82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **Available in 300 Mil DIP**

GENERAL DESCRIPTION

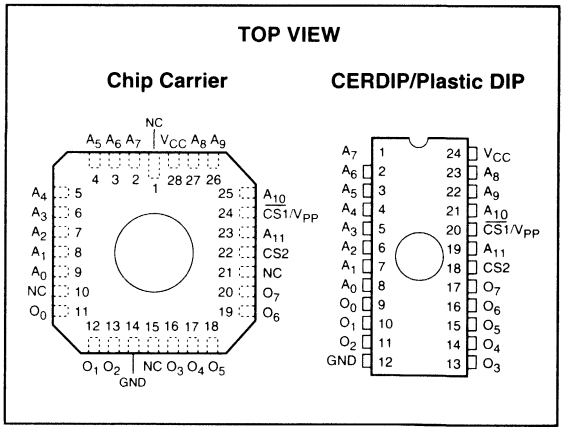
The WS57C43B is an extremely High Performance 32K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. A further advantage of the WS57C43B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C43B in a windowed package is 100% tested with worst case test patterns both before and after assembly.

The WS57C43B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

MODE SELECTION

PINS / MODE	$\overline{CS1}$/V_{PP}	CS2	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	V_{CC}	High Z
Output Disable	X	V_{IL}	V_{CC}	High Z
Program	V_{PP}	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C43B-35	WS57C43B-45	WS57C43B-55	WS57C43B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
CS to Output Valid Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Industrial		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

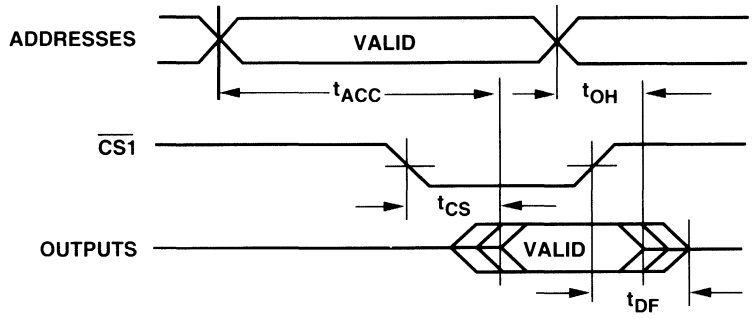
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C43B-35		57C43B-45		57C43B-55		57C43B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS1}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float*	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

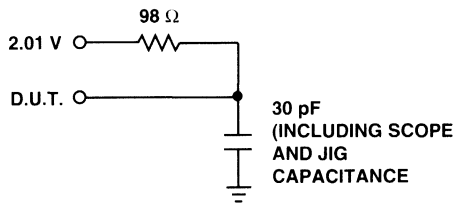


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

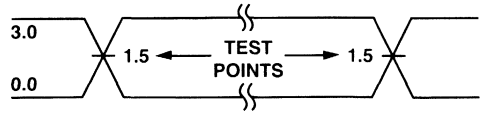
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

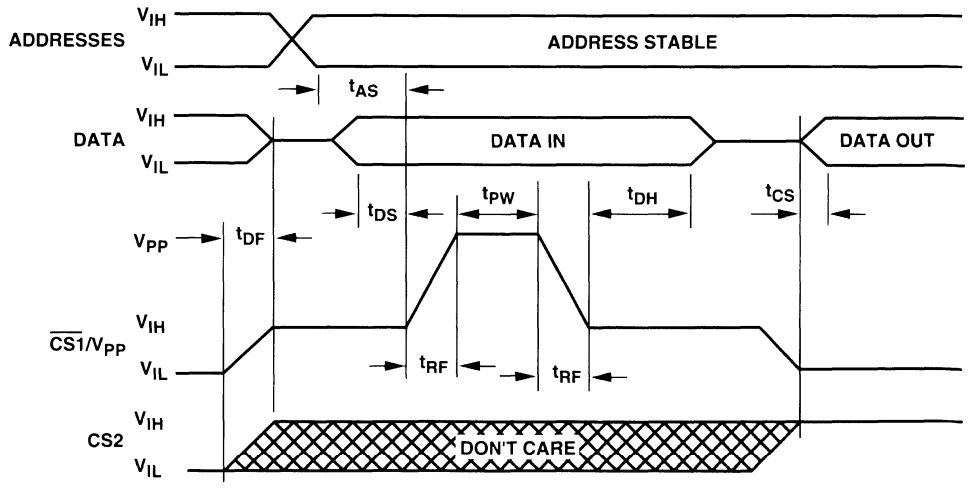
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current (Notes 2 and 3)		30	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTES: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-45CM	45	28 Pad CLLCC , 0.3"	C1	Military	Standard
WS57C43B-45CMB	45	28 Pad CLLCC , 0.3"	C1	Military	MIL-STD-883C
WS57C43B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C43B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43B-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-70TMB	70	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C43B is programmed using Algorithm A shown on page 5-3.

HIGH SPEED 4K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — t_{ACC} = 25 ns
  - — t_{CS} = 12 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with 4K x 8 Bipolar PROMs**
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000 V**
- **Available in 300 Mil DIP and PLDCC**

GENERAL DESCRIPTION

The WS57C43C is a High Performance 32K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. A further advantage of the WS57C43C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS5743C in a windowed package is 100% tested with worst case test patterns both before and after assembly.

The WS57C43C is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs, or its predecessor, the WS57C43B.

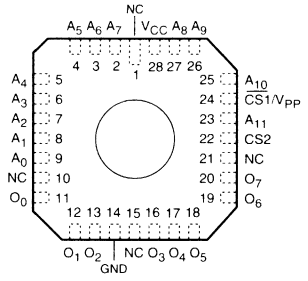
MODE SELECTION

PINS / MODE	$\overline{CS1}$ V_{PP}	CS2	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	V_{CC}	High Z
Output Disable	X	V_{IL}	V_{CC}	High Z
Program	V_{PP}	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{CC}	D_{OUT}

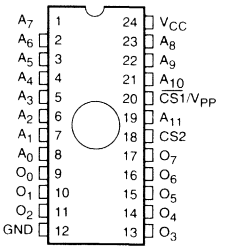
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	57C43C-25	57C43C-35	57C43C-45	57C43C-55	57C43C-70
Address Access Time (Max)	25 ns	35 ns	45 ns	55 ns	70 ns
CS to Output Valid Time (Max)	12 ns	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65° to + 150°C

Voltage on any Pin with Respect to Ground ..... −0.6V to +7V

V_{PP} with Respect to Ground ..... −0.6V to + 14V

ESD Protection ..... >2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Industrial		50	mA
			Military		50	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

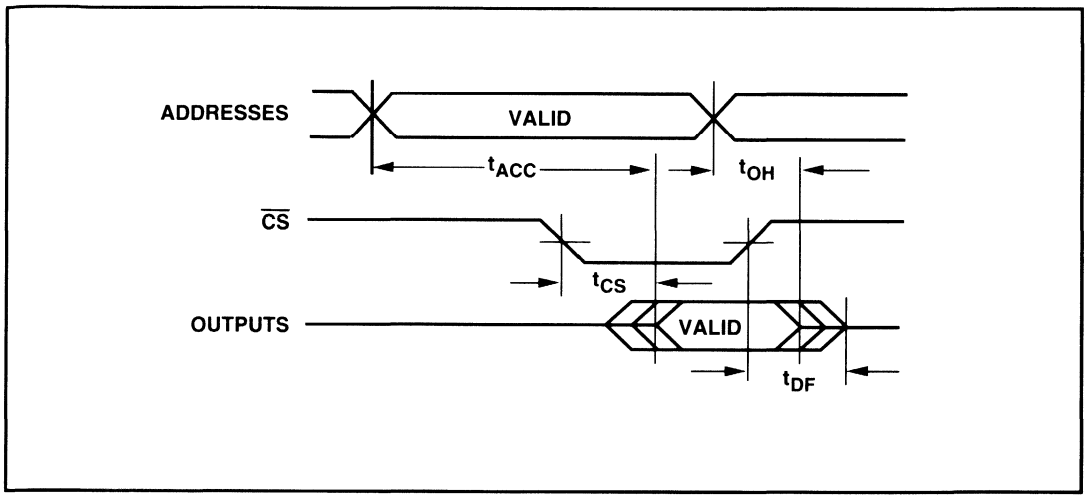
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C43C-25		57C43C-35		57C43C-45		57C43C-55		57C43C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		25		35		45		55		70	ns
$\overline{CS1}$ to Output Delay	t_{CS}		12		20		25		25		25	
Output Disable to Output Float*	t_{DF}		12		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

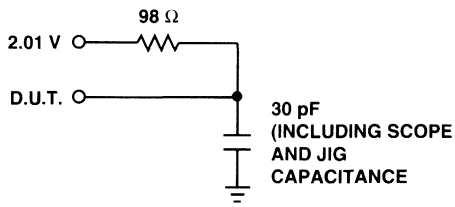


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

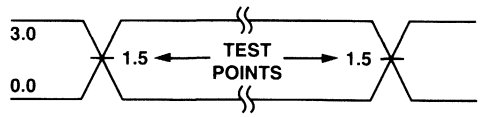
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

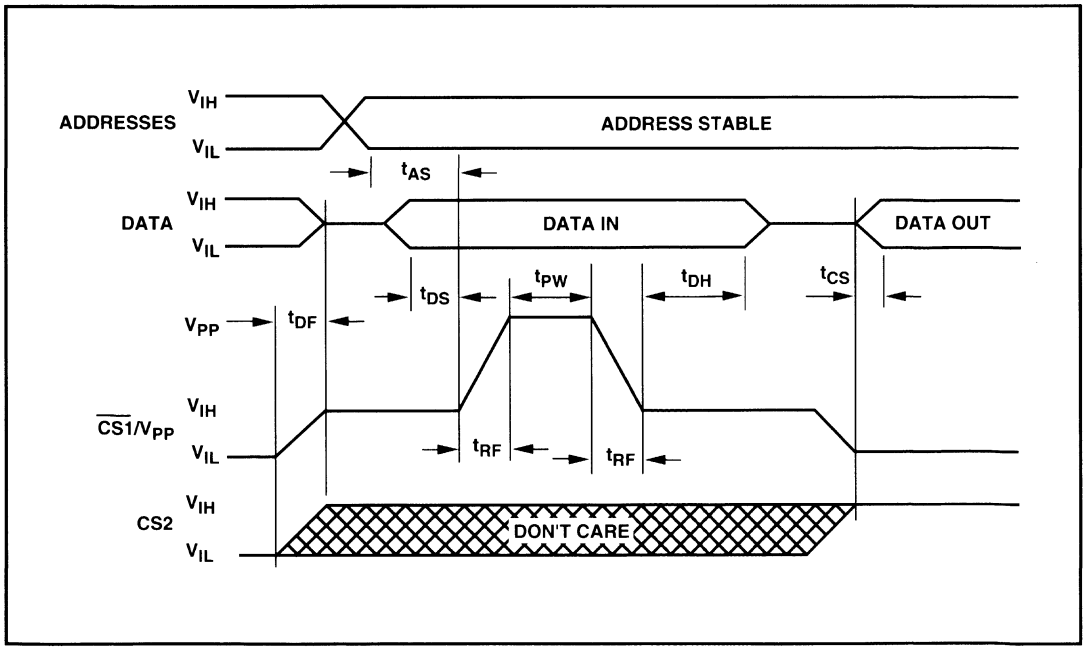
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		30	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTES: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43C-25D	25	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43C-25J	25	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43C-25S	25	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43C-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43C-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43C-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43C-35JI	35	28 Pin PLDCC	J3	Industrial	Standard
WS57C43C-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43C-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43C-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43C-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43C-45JI	45	28 Pin PLDCC	J3	Industrial	Standard
WS57C43C-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43C-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43C-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C43C-45TMB*	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43C-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43C-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43C-55TMB*	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43C-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43C-70TMB	70	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

*SMD product application in-process at DESC.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C43C is programmed using Algorithm D shown on page 5-7.

HIGH SPEED 8K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD 5962-87515**
- **Pin Compatible with Am27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000 V**

2

GENERAL DESCRIPTION

The WS57C49B is a High Performance 64K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. A further advantage of the WS57C49B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49B in a windowed package is 100% tested with worst case test patterns both before and after assembly.

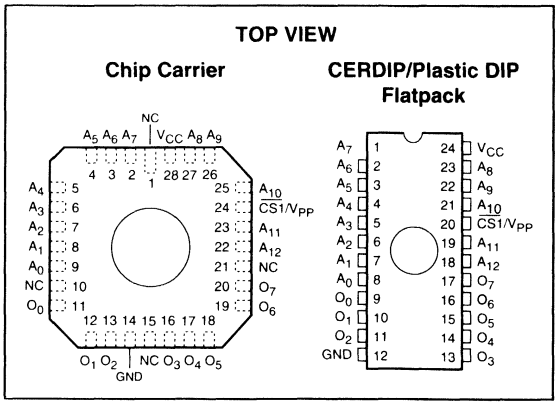
A unique feature of the WS57C49B is a designed-in output hold from address change. This enables the WS57C49B to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

MODE SELECTION

MODE \ PINS	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49B-35	WS57C49B-45	WS57C49B-55	WS57C49B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
CS to Output Valid Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....−65° to + 150°C

Voltage on any Pin with Respect to Ground .....−0.6V to +7V

V_{PP} with Respect to Ground.....−0.6V to + 14V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Industrial		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

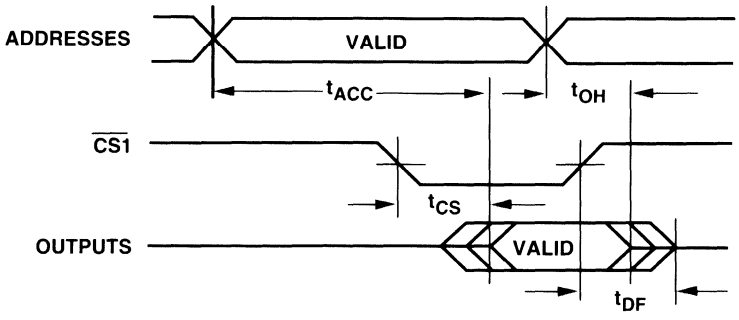
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C49B-35		57C49B-45		57C49B-55		57C49B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS1}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float*	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM



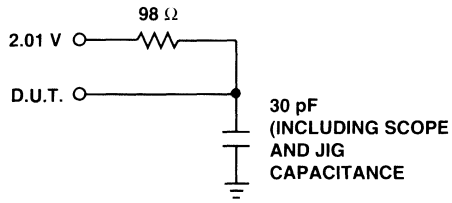
2

CAPACITANCE[5] T_A = 25°C, f = 1 MHz

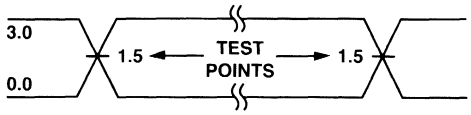
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

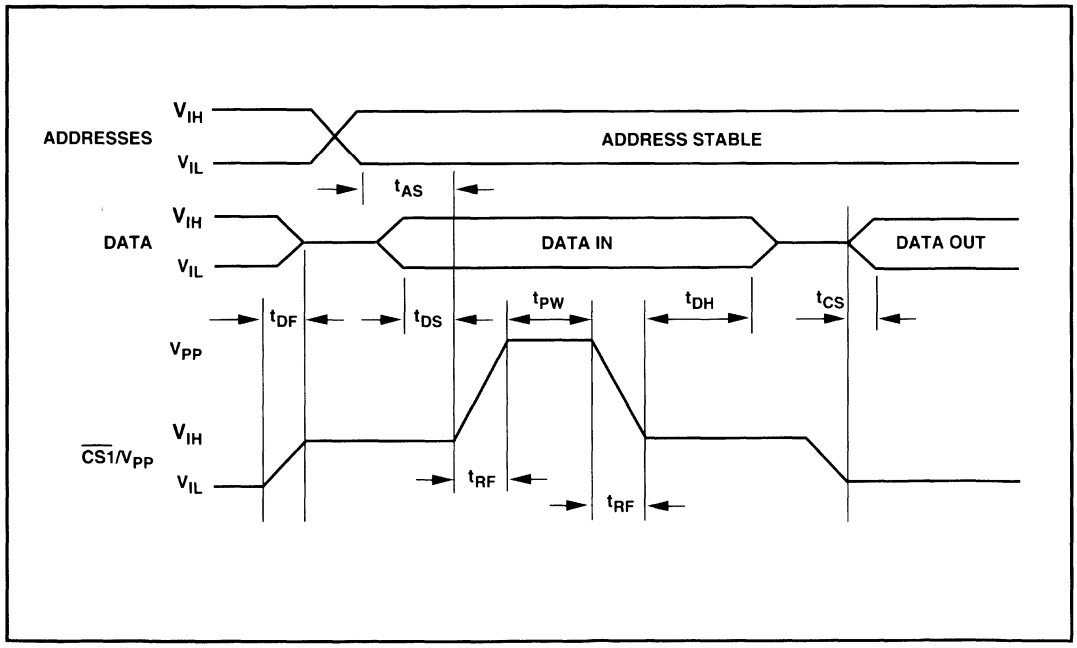
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4 mA)	2.4		V

NOTES: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-45CMB*	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-45FMB*	45	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-45DMB*	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-45JI	45	28 Pin PLDCC	J3	Industrial	Standard
WS57C49B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C49B-45TMB*	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49B-55CMB*	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-55DMB*	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-55FMB*	55	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49B-55J	55	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-55S	55	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-55TMB*	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49B-70CMB*	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-70DMB*	70	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-70T	70	28 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-70TMB*	70	28 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

*SMD product. See section 4 for SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C49B is programmed using Algorithm A shown on page 5-3.

HIGH SPEED 8K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - t_{ACC} = 25 ns
  - t_{CS} = 12 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with Bipolar PROMs**
- **Immune to Latch-UP**
  - Up to 200 mA
- **ESD Protection Exceeds 2000 V**
- **Available in 300 Mil DIP and PLDCC**

GENERAL DESCRIPTION

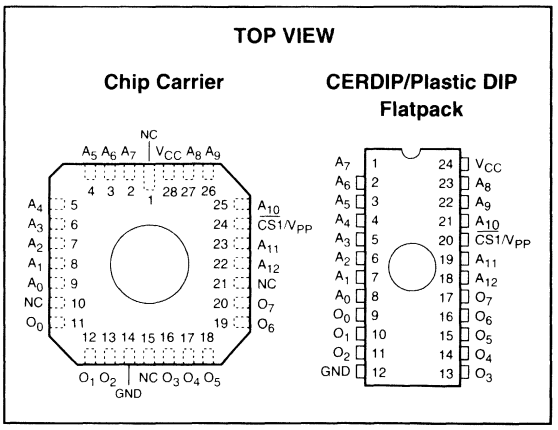
The WS57C49C is a High Performance 64K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. A further advantage of the WS57C49C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49C in a windowed package is 100% tested with worst case test patterns both before and after assembly.

The WS57C49C is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs, or its predecessor, the WS57C49B.

MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	57C49C-25	57C49C-35	57C49C-45	57C49C-55	57C49C-70
Address Access Time (Max)	25 ns	35 ns	45 ns	55 ns	70 ns
CS to Output Valid Time (Max)	12 ns	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65° to + 150°C

Voltage on any Pin with Respect to Ground ..... −0.6V to +7V

V_{PP} with Respect to Ground ..... −0.6V to + 13V

ESD Protection ..... >2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Industrial		50	mA
			Military		50	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

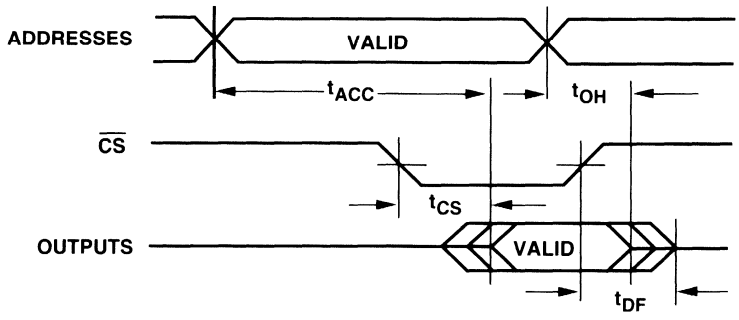
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C49C-25		57C49C-35		57C49C-45		57C49C-55		57C49C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		25		35		45		55		70	ns
$\overline{CS1}$ to Output Delay	t_{CS}		12		20		25		25		25	
Output Disable to Output Float*	t_{DF}		12		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

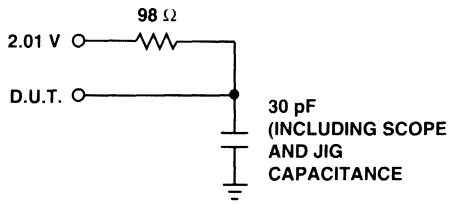


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

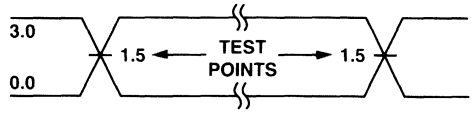
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

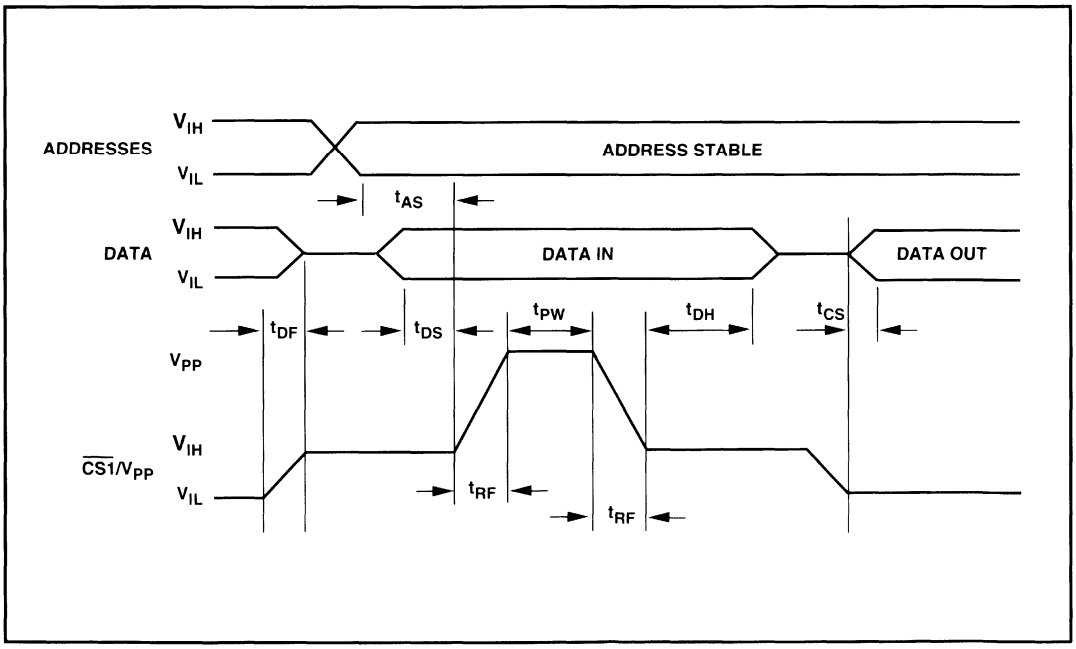
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4 mA)	2.4		V

NOTES: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49C-25D	25	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-25J	25	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-25S	25	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-35L	35	28 Pin CLDCC	L2	Comm'l	Standard
WS57C49C-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-35TI	35	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C49C-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49C-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49C-45FMB	45	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49C-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-45JI	45	28 Pin PLDCC	J3	Industrial	Standard
WS57C49C-45L	45	28 Pin CLDCC	L2	Comm'l	Standard
WS57C49C-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C49C-45TM	45	24 Pin CERDIP, 0.3"	T1	Military	Standard
WS57C49C-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49C-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49C-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49C-55FMB	55	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49C-55J	55	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-55S	55	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49C-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49C-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-70T	70	28 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-70TMB	70	28 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C49C is programmed using Algorithm D shown on page 5-7.

HIGH SPEED 16K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with Am27S51 and N82HS1281**
- **Immune to Latch-UP**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C51C is a High Performance 128K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

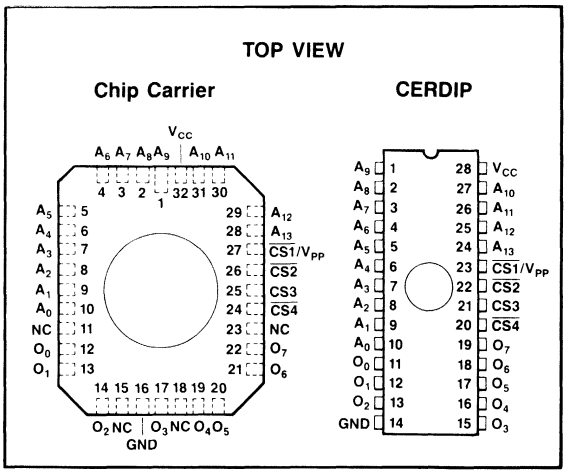
A further advantage of the WS57C51C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C51C in a windowed package is 100% tested with worst case test patterns both before and after assembly.

The WS57C51C provides a low power alternative to those designs which are committed to a Bipolar PROM footprint. It is a direct drop-in replacement for a Bipolar PROM of the same architecture (16K x 8). No software, hardware or layout changes need be performed.

MODE SELECTION

PINS / MODE	$\overline{CS1}$/V_{PP}	$\overline{CS2}$	CS3	$\overline{CS4}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	X	V_{CC}	High Z
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{IH}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	57C51C-35	57C51C-40	57C51C-45	57C51C-55	57C51C-70
Address Access Time (Max)	35 ns	40 ns	45 ns	55 ns	70 ns
CS to Output Valid Time (Max)	20 ns	20 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		50	mA
			Industrial		60	mA
			Military		60	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

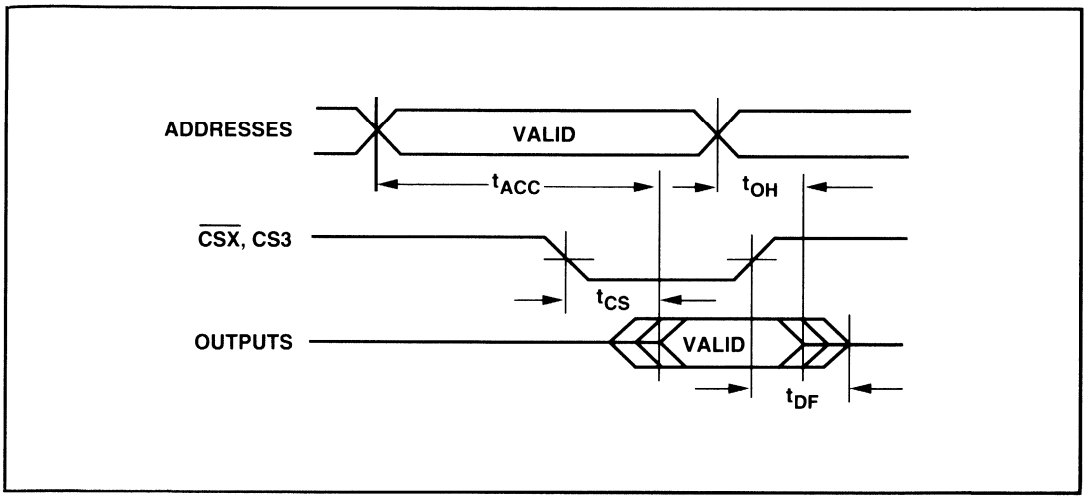
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 4 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C51C-35		57C51C-40		57C51C-45		57C51C-55		57C51C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		40		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20		25		30	
Output Disable to Output Float*	t_{DF}		20		20		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

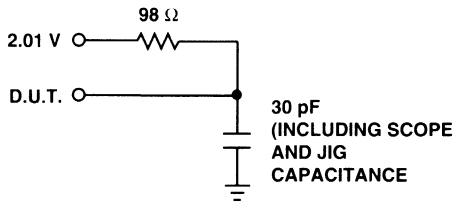


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

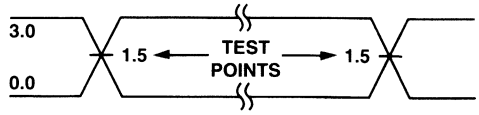
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

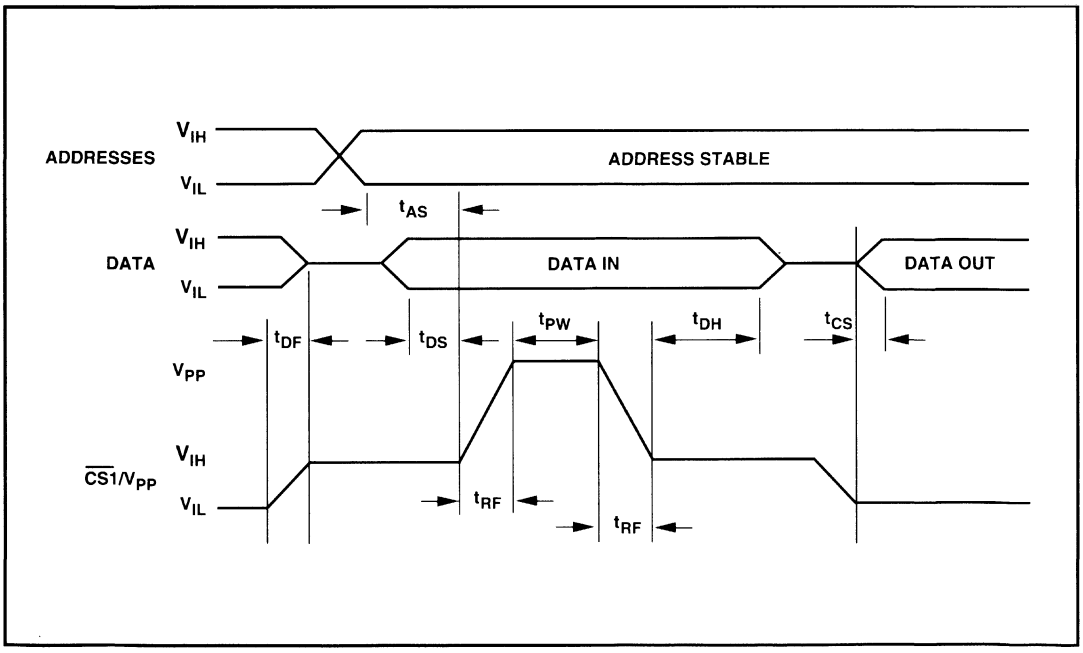
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTE: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width (Note 7)	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C51C-35D	35	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51C-35TI	35	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51C-45CMB	45	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51C-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-45DMB	45	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51C-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51C-45JI	45	32 Pin PLDCC	J4	Industrial	Standard
WS57C51C-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51C-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51C-45TI	45	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51C-45TMB	45	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C51C-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51C-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51C-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51C-55JI	55	32 Pin PLDCC	J4	Industrial	Standard
WS57C51C-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51C-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51C-55TI	55	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51C-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C51C-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

NOTE: The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C51C is programmed using Algorithm D shown on page 5-7.

HIGH SPEED 32K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Available in 300 Mil DIP and PLDCC**

GENERAL DESCRIPTION

The WS57C71C is a High Performance 256K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology and utilizes WSI's patented self-aligned split gate EPROM cell.

The industry standard PROM pin configuration of the WS57C71C provides an easy upgrade path from a 16K x 8 device as well as providing a future upgrade path to 64K x 8 and 128K x 8 devices.

This RPROM is capable of operating at speeds as fast as 35 ns address access time, which enables it to be used directly with today's fast microprocessors and DSP processors without introducing any wait states. All inputs and outputs are TTL compatible. The WS57C71C is a low power device even when operated at its fastest speed. The DIP version is packaged in a 300 mil wide DIP package saving board space for the user.

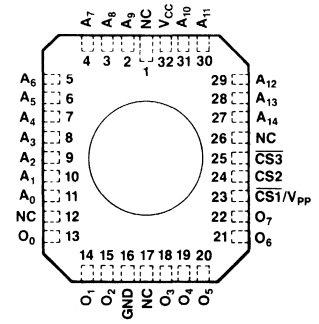
MODE SELECTION

PINS / MODE	$\overline{CS1}$/V_{PP}	CS2	$\overline{CS3}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	X	V_{IH}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Program Inhibit	V_{PP}	X	V_{IL}	V_{CC}	High Z

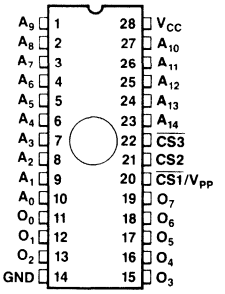
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



NOTE:
J-Package (PLDCC) only: Pins No. 1 and 17 are common and tied to the die attach pad. They must therefore be D.U. (don't use or float) or tied to GND.

PRODUCT SELECTION GUIDE

PARAMETER	WS57C71C-35	WS57C71C-45	WS57C71C-55	WS57C71C-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
CS to Output Valid Time (Max)	15 ns	20 ns	20 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 13V

ESD Protection.....>2000V

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		50	mA
			Industrial		60	mA
			Military		60	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

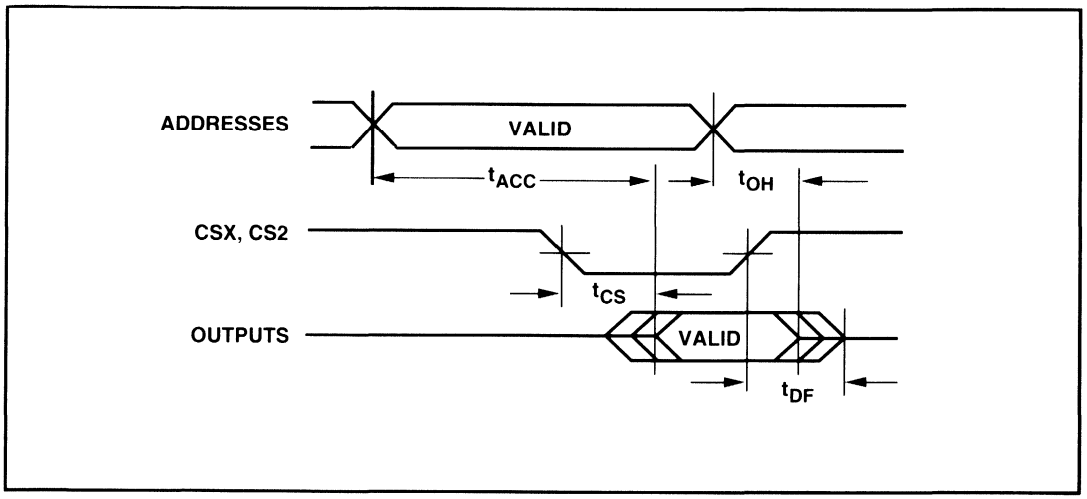
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C71C-35		57C71C-45		57C71C-55		57C71C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		15		20		20		30	
Output Disable to Output Float*	t_{DF}		20		20		20		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

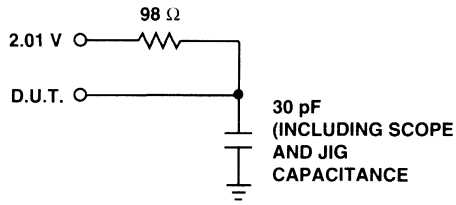


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

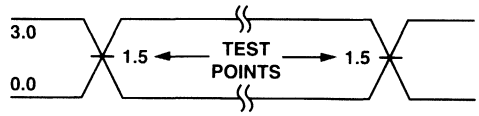
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

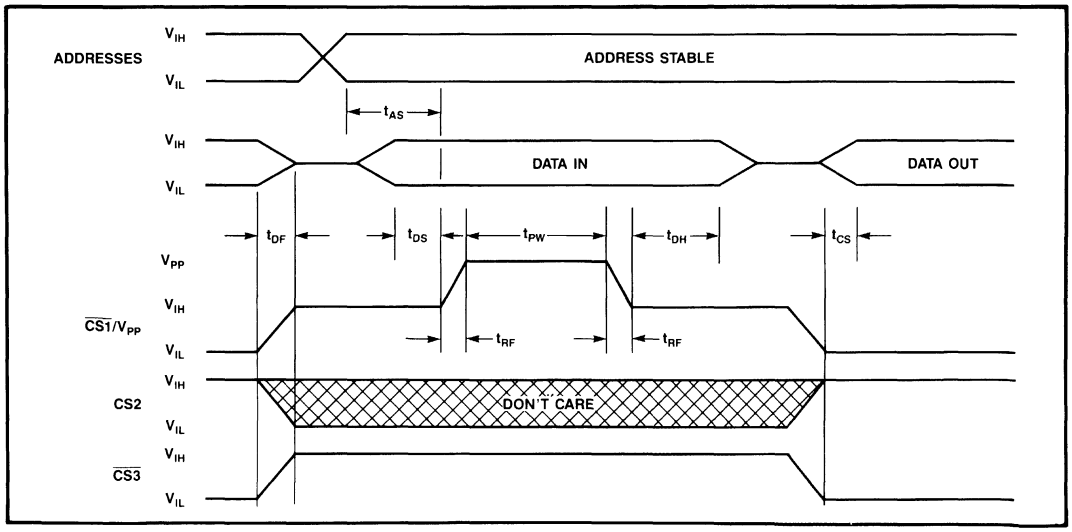
PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	–10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = –4 mA)	V_{OH}	2.4		V

NOTES: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C71C-35J	35	32 Pin PLDCC	J4	Comm'l	Standard
WS57C71C-35L	35	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-45CI	45	32 Pad CLLCC	C2	Industrial	Standard
WS57C71C-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C71C-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C71C-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C71C-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C71C-55JI	55	32 Pin PLDCC	J4	Industrial	Standard
WS57C71C-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-55TI	55	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C71C-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C71C-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-70L	70	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-70TMB	70	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C

NOTE: 9. The actual part marking will not include the initials "WS."

2

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C71C is programmed using Algorithm D shown on page 5-7.

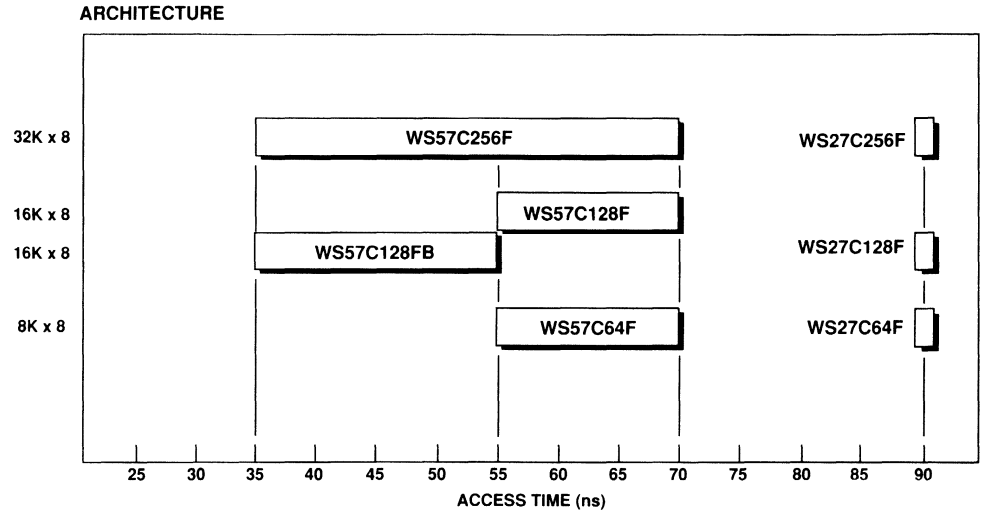
Section Index

EPROM Memory Products

FAMILY OF HIGH PERFORMANCE CMOS EPROMs

PART NUMBER	PAGE NO.	DENSITY (BITS)	ARCHITECTURE	SPEED (ns)	DRAWING NO.	NO. OF PINS	PACKAGE
WS57C64F	3-7	64K	8K x 8	55–70	C2 D2 J4	32 28 32	CLLCC CERDIP, 0.6" PLDCC
WS27C64F	3-13	64K	8K x 8	90	C2 D2	32 28	CLLCC CERDIP, 0.6"
WS57C128F	3-19	128K	16K x 8	55–70	C2 D2	32 28	CLLCC CERDIP, 0.6"
WS57C128FB	3-25	128K	16K x 8	35–55	C2 D2 J4 L3	32 28 32 32	CLLCC CERDIP, 0.6" PLDCC CLDCC
WS27C128F	3-31	128K	16K x 8	90	C2 D2	32 28	CLLCC CERDIP, 0.6"
WS57C256F	3-37	256K	32K x 8	35–70	C2 D2 J4 L3 P3 T2	32 28 32 32 28 28	CLLCC CERDIP, 0.6" PLDCC CLDCC Plastic DIP 0.6" CERDIP, 0.3"
WS27C256F	3-43	256K	32K x 8	90	C2 D2 L3	32 28 32	CLLCC CERDIP, 0.6" CLDCC

WSI's Family of High Performance CMOS EPROMs are available in all three operating temperature ranges: Commercial (0 to +70°C), Industrial (–40 to +85°C) and Military (–55 to +125°C). In addition, several versions are available as Standard Military Drawing (SMD) products.


ARCHITECTURE
32K x 8
16K x 8
16K x 8
8K x 8
WS57C256F
WS57C128F
WS57C128FB
WS57C64F
WS27C256F
WS27C128F
WS27C64F
25
30
35
40
45
50
55
60
65
70
75
80
85
90
ACCESS TIME (ns)

AMD	WSI
Am27C128	WS57C128FB
Am27C256	WS57C256F
Am27C64	WS57C64F
Am27H256	WS57C256F

ATMEL	WSI
AT27HC256/L	WS57C256F
AT27HC256R/R	WS57C256F
AT27HC64/L	WS57C64F
AT27HC64R/RL	WS57C64F

CATALYST	WSI
CAT27128A	WS57C128FB
CAT27256	WS57C256F
CAT2764A	WS57C64F
CAT27HC256	WS57C256F

CYPRESS	WSI
CY7C274	WS57C256F

HITACHI	WSI
HN27C256HG	WS57C256F

INTEL	WSI
27C128B	WS57C128FB
27C256	WS57C256F

MICROCHIP	WSI
27HC256	WS57C256F
27HC64	WS57C64F

OKI	WSI
MSM27C256	WS57C256F

SANYO	WSI
LA7620	WS57C64F

SGS-T	WSI
M27128/A	WS57C128FB
M27256	WS57C256F
TS27C64A	WS57C64F

SHARP	WSI
LH57126	WS57C128FB
LH5763	WS57C64F
LH5762	WS57C64F

SIGNETICS	WSI
27HC128	WS57C128FB

TI	WSI
TMS27C64	WS57C64F
TMS27C128	WS57C128FB

TOSHIBA	WSI
TMM27128`	WS57C128FB
TMM27256	WS57C256F
TMM2764	WS57C64F

HIGH SPEED 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 85102**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Available in PLDCC**

GENERAL DESCRIPTION

The WS57C64F is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming very little power.

Two major features of the WS57C64F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include modems, secure telephones, servo controllers, and industrial controllers.

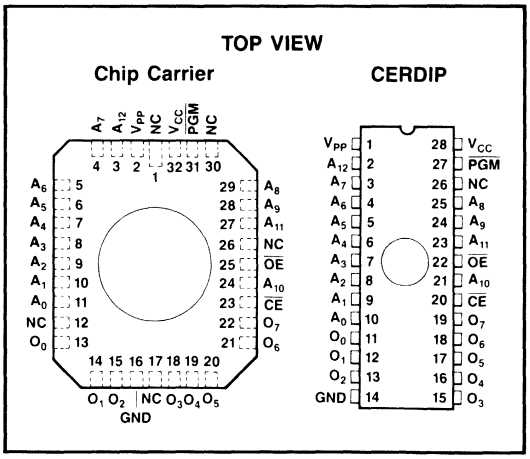
The WS57C64F is configured in the standard EPROM pinout which provides an easy upgrade path to higher density EPROMs.

3

MODE SELECTION

PINS / MODE	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	X	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	V_{CC}	High Z

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C64F-55	WS57C64F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	20ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....−65° to + 150°C

Voltage on any Pin with Respect to Ground .....−0.6V to +7V

V_{PP} with Respect to Ground.....−0.6V to + 14V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

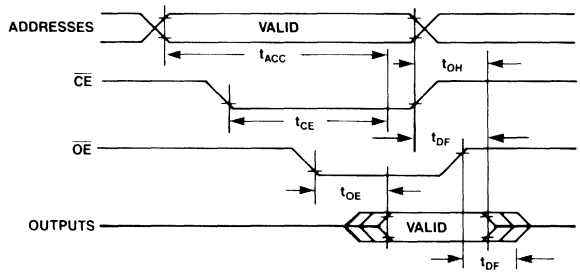
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3 V (Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH} (Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		20	mA
			Industrial		30	mA
			Military		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		25	mA
			Industrial		35	mA
			Military		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

PARAMETER	SYMBOL	WS57C64F-55		WS57C64F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		20		25	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM

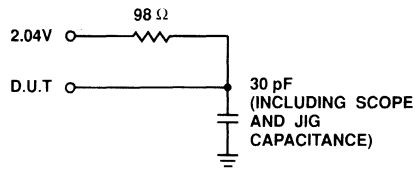


CAPACITANCE[6] T_A = 25°C, f = 1 MHz

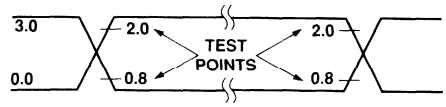
SYMBOL	PARAMETER	CONDITIONS	TYP[7]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

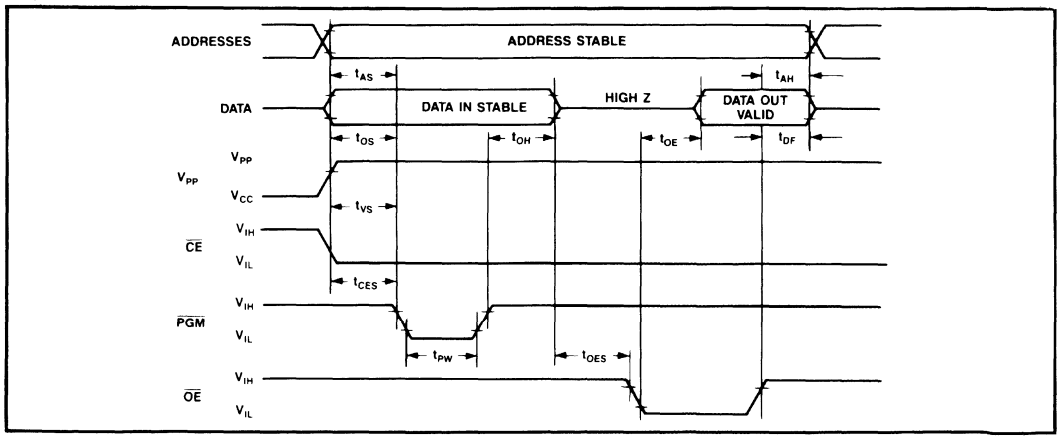
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C64F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C64F-70CMB*	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C64F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C64F-70DMB*	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C64F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard

NOTES: 12. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C64F is programmed using Algorithm A shown on page 5-3.

MILITARY 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 85102**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Military Temperature Operating Range**

GENERAL DESCRIPTION

The WS27C64F is a High Performance 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full Military temperature operating range.

The WS27C64F is a direct drop-in replacement for the industry standard 27C64 and/or 2764 EPROMs. It was developed specifically for this purpose and requires no board or software modifications to complete the change.

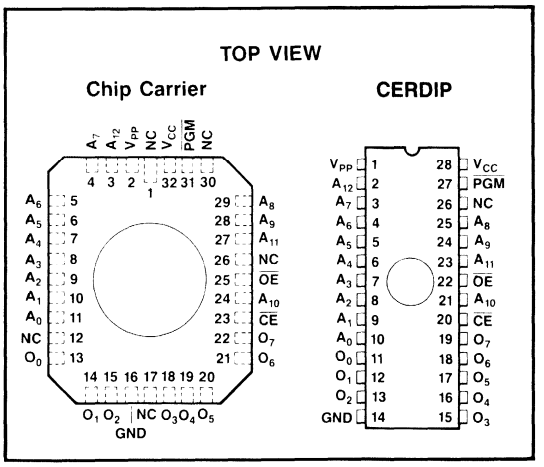
The WS27C64F is configured in the standard EPROM pinout which provides an easy upgrade path to the WS27C128F and WS27C256F.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. $A_0 = V_{IL}$ = MFGR 23H, $A_0 = V_{IH}$ = DEVICE A8H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C64F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65° to +150°C
Voltage on Any Pin with
Respect to GND ..... −0.6V to +7V
V_{PP} with respect to GND ..... −0.6V to +14V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

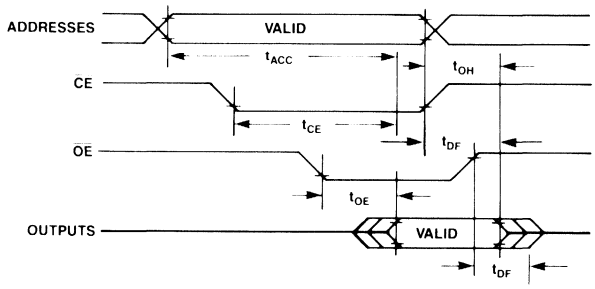
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Note 1)		200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Note 2)		10	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		25	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C64F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

AC READ TIMING DIAGRAM

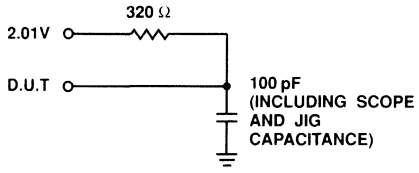


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

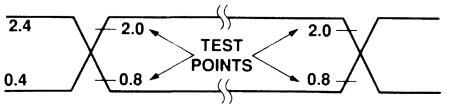
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

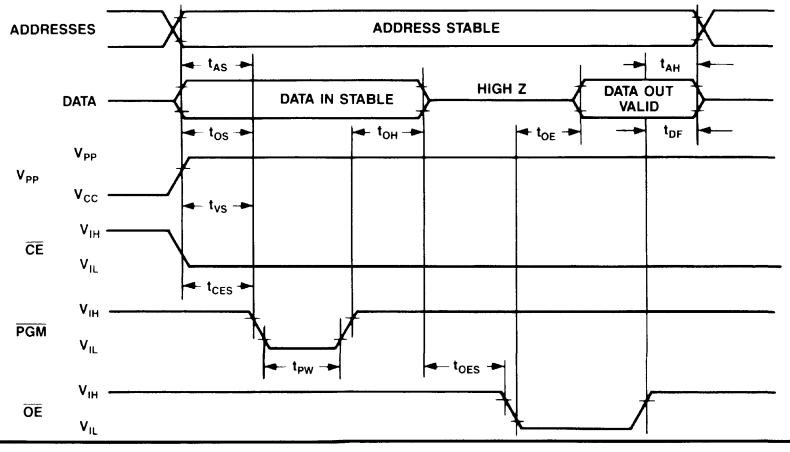
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current (Note 3)		50	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 4 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 1mA)	2.4		V

NOTES: 8. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
9. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
10. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C64F-90CMB*	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-90DMB*	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTES: 11. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS27C64F is programmed using Algorithm A shown on page 5-3.

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS57C128F is a High Performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at Bipolar speeds while consuming only 90 mA.

Two major features of the WS57C128F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

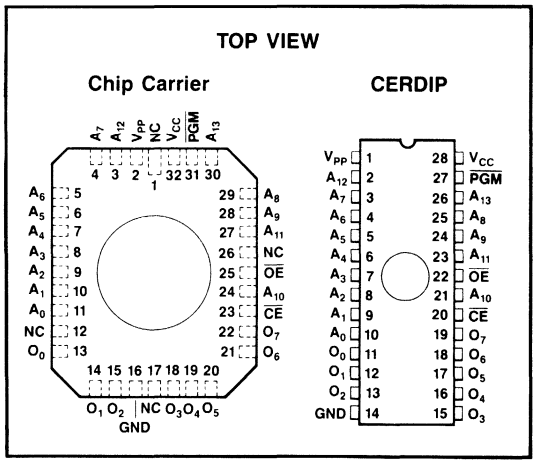
The WS57C128F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

PINS / MODE	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	X	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	V_{CC}	High Z

X can be V_{IL} or V_{IH}.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C128F-55	WS57C128F-70
Address Access Time (Max)	55 ns	70 ns
Chip Select Time (Max)	55 ns	70 ns
Output Enable Time (Max)	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

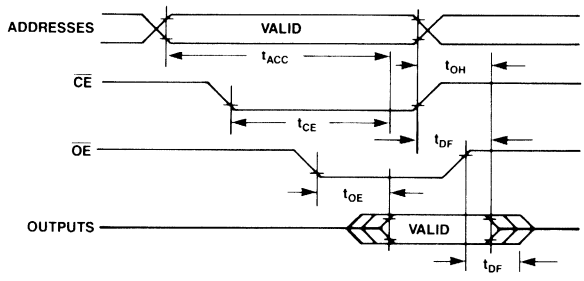
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4)	Comm'l		30	mA
		Outputs Not Loaded	Military		40	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4)	Comm'l		50	mA
		Outputs Not Loaded	Military		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 4 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS57C128F-55		WS57C128F-70		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay		55		70	
t_{OE}	$\overline{OE}$ to Output Delay		25		25	
t_{DF}	Output Disable to Output Float		25		25	
t_{OH}	Address to Output Hold	0		0		

AC READ TIMING DIAGRAM

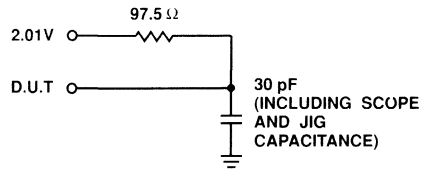


CAPACITANCE[6] T_A = 25°C, f = 1 MHz

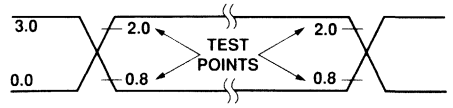
SYMBOL	PARAMETER	CONDITIONS	TYP[7]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

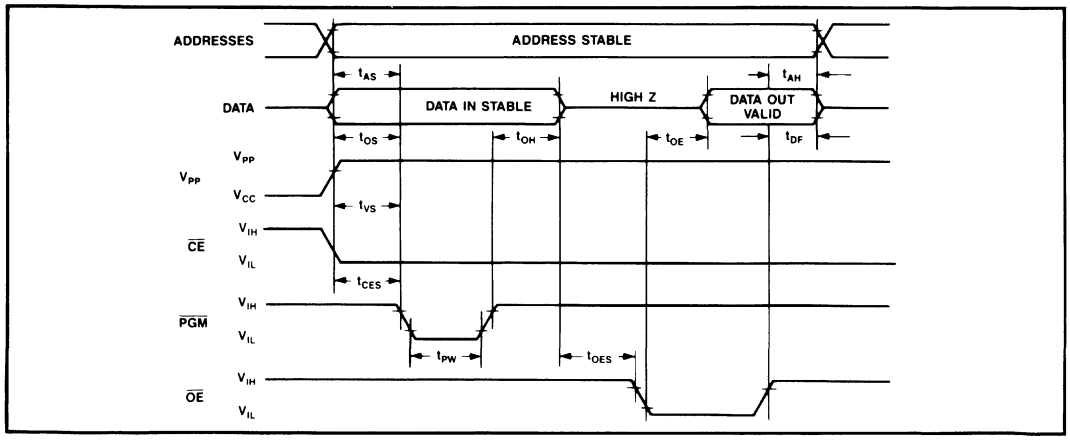
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		30	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

NOTES:
9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C128F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C128F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C128F-70DM	70	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C128F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTES: 12. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C128F is programmed using Algorithm A shown on page 5-3.

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **DIP and Surface Mount Packaging Available**

GENERAL DESCRIPTION

The WS57C128FB is a High Performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at Bipolar speeds while consuming only 90 mA.

Two major features of the WS57C128FB are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited.

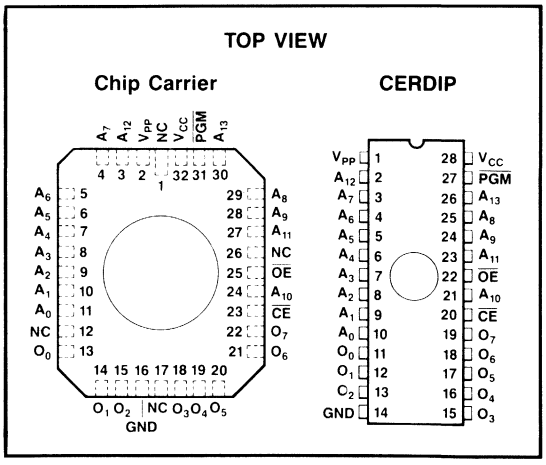
The WS57C128FB is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs. The EPROMs are available in both 600 Mil Dip packages, and both J-leaded and leadless surface mount packages.

MODE SELECTION

PINS / MODE	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	X	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	V_{CC}	High Z

X can be V_{IL} or V_{IH}.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C128FB-35	WS57C128FB-45	WS57C128FB-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Chip Select Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....−65° to + 150°C

Voltage on any Pin with Respect to Ground .....−0.6V to +7V

V_{PP} with Respect to Ground.....−0.6V to + 13V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

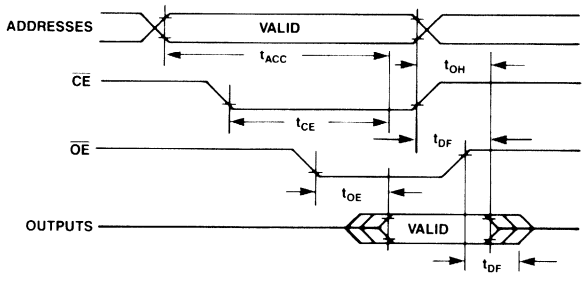
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		30	mA
			Industrial		40	mA
			Military		40	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		50	mA
			Industrial		60	mA
			Military		60	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 4 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

PARAMETER	SYMBOL	57C128FB-35		57C128FB-45		57C128FB-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
$\overline{CE}$ to Output Delay	t_{CE}		35		45		55	
$\overline{OE}$ to Output Delay	t_{OE}		20		25		25	
Output Disable to Output Float	t_{DF}		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM

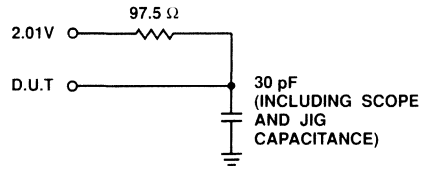


CAPACITANCE (6) T_A = 25°C, f = 1 MHz

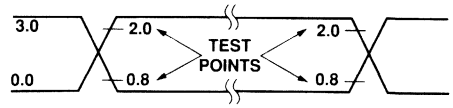
SYMBOL	PARAMETER	CONDITIONS	TYP (7)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

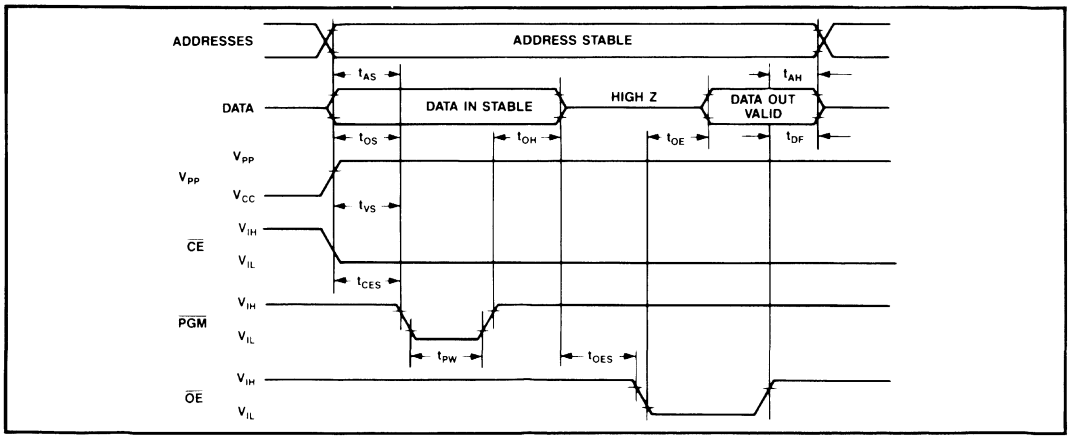
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		30	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4mA)	2.4		V

NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either concident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C128FB-35D	35	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128FB-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128FB-45DMB	45	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C128FB-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C128FB-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C128FB-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C128FB-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: 12. The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C128FB is programmed using Algorithm D shown on page 5-7.

MILITARY 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Military Operating Range**

GENERAL DESCRIPTION

The WS27C128F is an extremely High Performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full military temperature operating range.

The WS27C128F was specifically designed to replace standard EPROMs in military environments. No hardware or software changes are required to replace standard military 27128 EPROMs with the WSI WS27C128F.

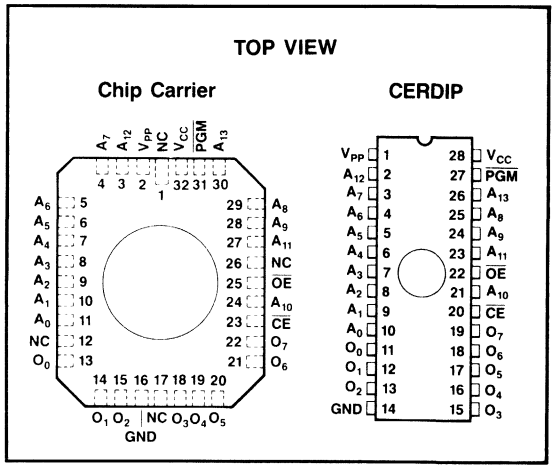
The WS27C128F is configured in the standard EPROM pinout which provides an easy upgrade path for the WS27C64F.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C128F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	− 0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = − 1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Note 1)		200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Note 2)		10	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		25	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

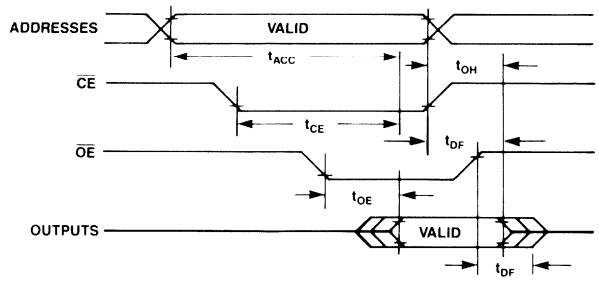
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C128F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

NOTE: 5. Single shot programming algorithms should use one 10 ms PGM pulse per word.

AC READ TIMING DIAGRAM

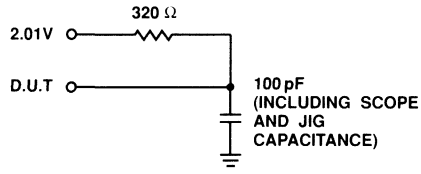


CAPACITANCE[6] T_A = 25°C, f = 1 MHz

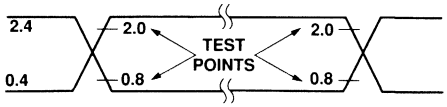
SYMBOL	PARAMETER	CONDITIONS	TYP[7]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

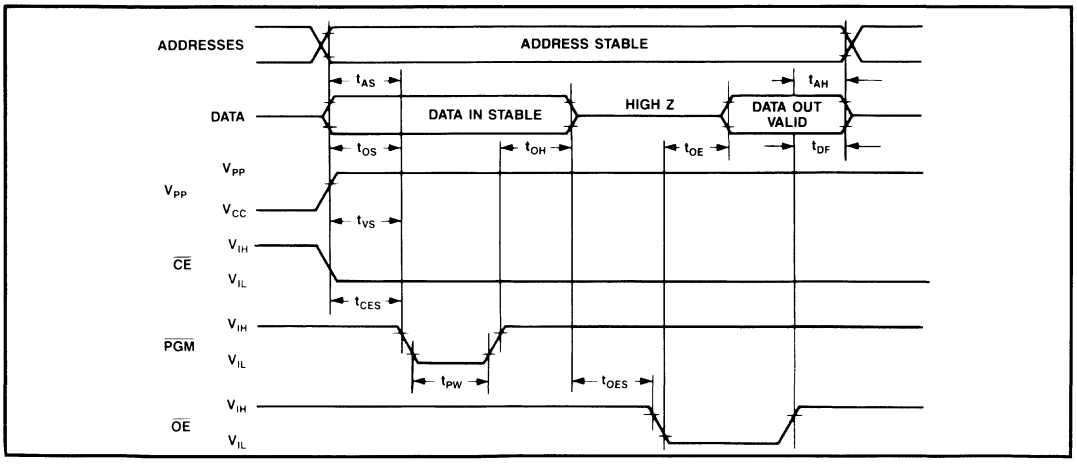
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		30	mA
I_{CC}	V_{CC} Supply Current		50	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 4 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 1mA)	2.4		V

NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	5		ms

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C128F-90CMB*	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C128F-90DM	90	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS27C128F-90DMB*	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS27C128F is programmed using Algorithm A shown on page 5-3.

HIGH SPEED 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  — Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS57C256F is a High Performance 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at speeds as fast as 35 ns Access Time.

Two major features of the WS57C256F are its Low Power and High Speed. While operating in a TTL environment it consumes only 120 mA while cycling at full speed. Additionally, the WS57C256F can be placed in a standby mode which drops operating current below 15 mA in a TTL environment and 500 µA in a CMOS environment.

The WS57C256F also has exceptional output drive capability. It can source 4 mA and sink 16 mA per output.

The WS57C256F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

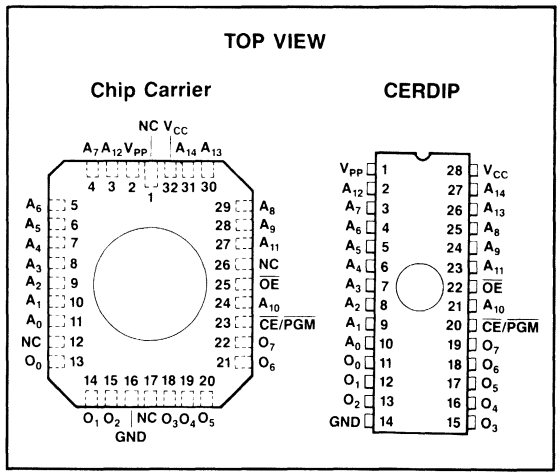
MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	X	V_{PP}[2]	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	X	X	V_{PP}[2]	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	V_{PP}[2]	V_{CC}	High Z
Signature[3]	V_{IL}	V_{IL}	V_H[2]	V_{IL}	V_{CC}	V_{CC}	23 H[4]
	V_{IL}	V_{IL}	V_H[2]	V_{IH}	V_{CC}	V_{CC}	EO H[5]

NOTES:

1. X can be V_{IL} or V_{IH}.
2. $V_H = V_{PP} = 12.75 \pm 0.25V$.
3. A_1–A_8, A_{10}–$A_{14} = V_{IL}$.
4. Manufacturer
5. Device

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C256F-35	WS57C256F-45	WS57C256F-55	WS57C256F-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	15 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 13V

ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

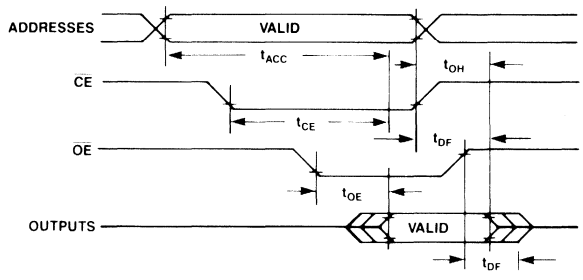
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Level	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3 V (Note 1)			200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH} (Note 2)			3	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		25	mA
			Industrial		30	mA
			Military		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		50	mA
			Industrial		60	mA
			Military		60	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} –0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. with $V_{PP} = V_{CC}$

PARAMETER	SYMBOL	57C256F-35		57C256F-45		57C256F-55		57C256F-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		40		45		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		15		20		25		30	
Output Disable to Output Float	t_{DF}		20		20		25		30	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM

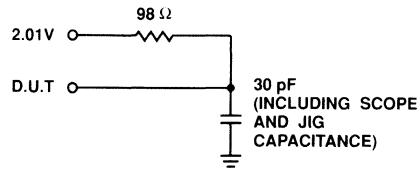


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

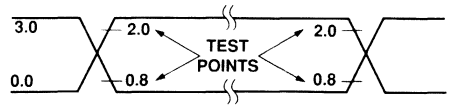
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6.Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

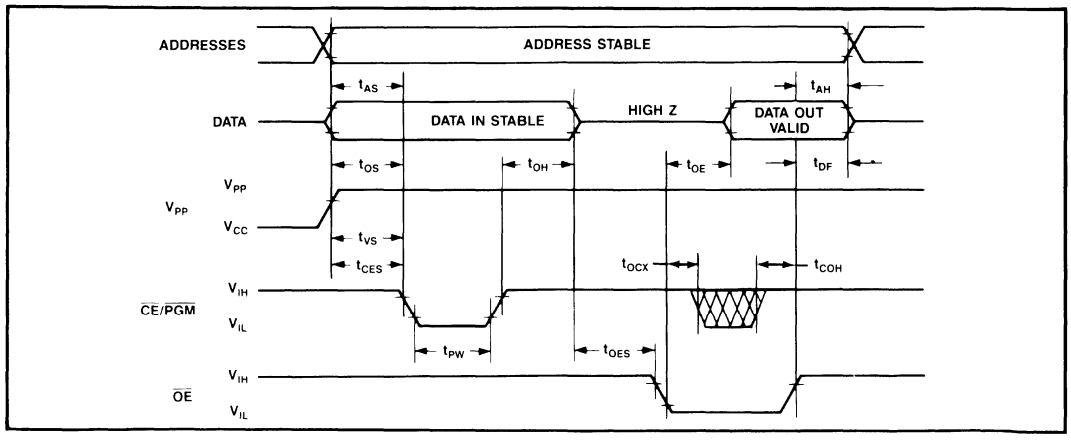
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current (Note 4)		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4mA)	2.4		V

NOTES:
9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched fromm 5 volts to 12.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{COH}	$\overline{CE}$ High to $\overline{OE}$ High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	0.1	1	10	ms
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C256F-35D	35	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-35J	35	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-35P	35	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS57C256F-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-45C	45	32 Pad CLLCC	C2	Comm'l	Standard
WS57C256F-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C256F-45P	45	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS57C256F-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-55C	55	32 Pad CLLCC	C2	Comm'l	Standard
WS57C256F-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-55JI	55	32 Pin PLDCC	J4	Industrial	Standard
WS57C256F-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C256F-55P	55	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS57C256F-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C256F-70CM	70	32 Pad CLLCC	C2	Military	Standard
WS57C256F-70CMB*	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C256F-70DM	70	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C256F-70DMB*	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-70JI	70	32 Pin PLDCC	J4	Industrial	Standard
WS57C256F-70LMB	70	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C256F-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

NOTES: 12. The actual part marking will not include the initials "WS."
13. Shaded area describes newest product. Contact your WSI Sales Representative for availability.

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C256F is programmed using Algorithm D shown on page 5-7.

MILITARY 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  - — Latch-up Immunity Up to 200 mA
  - — ESD Protection Exceeds 2000V
- **Standard EPROM Pinout**
- **Military Operating Range**

GENERAL DESCRIPTION

The WS27C256F is an extremely High Performance 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full military temperature operating range.

The WS27C256F was specifically designed to replace standard EPROMs in military environments. No hardware or software changes are required to replace standard military 27256 EPROMs with the WSI WS27C256F.

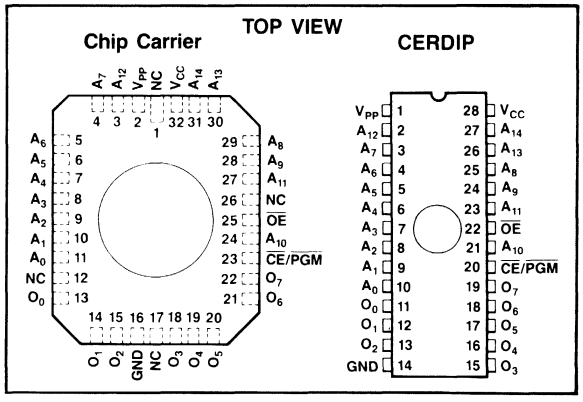
The WS27C256F is configured in the standard EPROM pinout which provides an easy upgrade path from the WS27C64F, and the 128K Bit WS27C128F.

MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

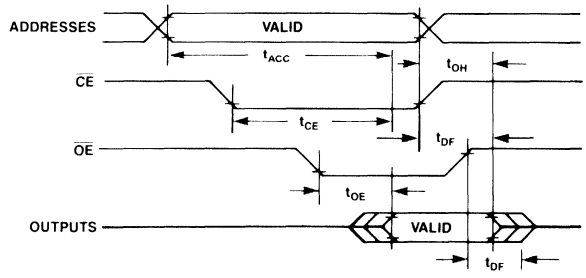
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ (Note 1)		500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$ (Note 2)		5	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		40	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		45	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C256F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

AC READ TIMING DIAGRAM

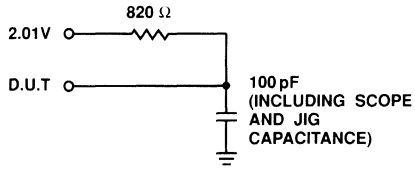


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

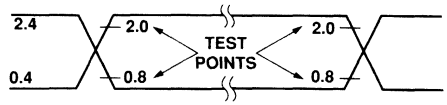
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

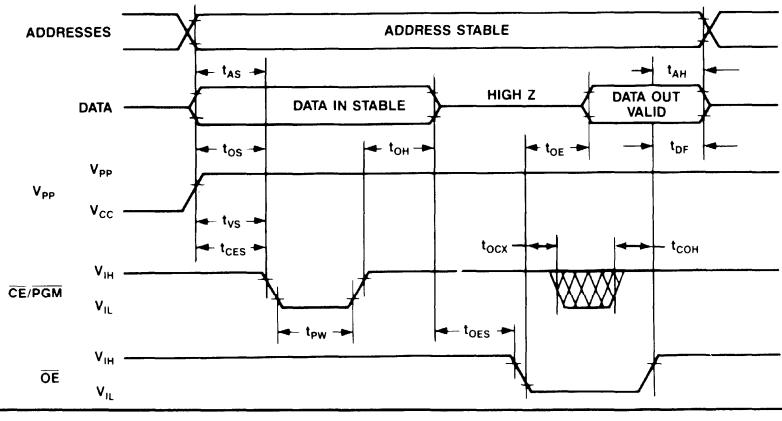
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ / $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

NOTES: 8. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
9. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
10. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{COH}	$\overline{CE}$ High to $\overline{OE}$ High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-90CMB*	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-90DMB*	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-90LMB	90	32 Pin CLDCC	L3	Military	MIL-STD-883C

NOTE: 11. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS27C256F is programmed using Algorithm B shown on page 5-5.

Section Index

Standard Military Drawing (SMD) Selector Guide

For additional information,
Call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363

Standard Military Drawing (SMD) Selector Guide

Product Number

WSI supports the Standardized Military Drawings (SMD) program sponsored by the Defense Electronics Supply Center (DESC), Dayton, Ohio 45444-5277. Copies of the SMD may be obtained by calling DESC at Tel: (513) 296-6095.

SMD Part Number	WSI Part Number
5962-8606301XA	WS27C256L-20DMB
5962-8606301YC	WS27C256L-20CMB
5962-8606301UX	WS27C256L-20TMB
5962-8606302XA	WS27C256L-25DMB
5962-8606302YC	WS27C256L-25CMB
5962-8606305XA	WS27C256L-15DMB
5962-8606305YC	WS27C256L-15CMB
5962-8606305UX	WS27C256L-15TMB
5962-8606306XA	WS27C256L-12DMB
5962-8606306YC	WS27C256L-12CMB
5962-8606306UX	WS27C256L-15TMB
5962-8606307XA	WS27C256F-90DMB
5962-8606307YC	WS27C256F-90CMB
5962-8606308XA	WS57C256F-70DMB
5962-8606308YC	WS57C256F-70CMB
5962-8751501JA	WS57C49B-45DMB
5962-8751501KA	WS57C49B-45FMB
5962-8751501LA	WS57C49B-45TMB
5962-87515013C	WS57C49B-45CMB
5962-8751502JA	WS57C49B-55DMB
5962-8751502KA	WS57C49B-55FMB
5962-8751502LA	WS57C49B-55TMB
5962-87515023C	WS57C49B-55CMB
5962-8751503JA	WS57C49B-70DMB
5962-8751503LA	WS57C49B-70TMB
5962-87515033C	WS57C49B-70CMB
5962-8751504LA	WS57C49B-90TMB
5962-8752901KA	WS57C45-45FMB
5962-8752901LA	WS57C45-45TMB
5962-87529013C	WS57C45-45CMB
5962-8752902KA	WS57C45-35FMB
5962-8752902LA	WS57C45-35TMB
5962-87529023C	WS57C45-35CMB

Product Number (Cont.)

SMD Part Number	WSI Part Number
5962-8764801XA	WS27C512L-15DMB
5962-8764801YC	WS27C512L-15CMB
5962-8764802XA	WS27C512L-20DMB
5962-8764802YC	WS27C512L-20CMB
5962-8764804XA	WS27C512L-12DMB
5962-8764804YC	WS27C512L-12CMB
5962-8765001JA	WS57C191B-50DMB
5962-8765001LA	WS57C291B-50TMB
5962-87650013C	WS57C191B-50CMB
5962-8765002JA	WS57C191B-55DMB
5962-8765002LA	WS57C291B-55TMB
5962-8765004JA	WS57C191B-45DMB
5962-8765004LA	WS57C291B-45TMB
5962-87650043C	WS57C191B-45CMB
5962-8765004KA	WS57C191B-45FMB
5962-88734013C	WS57C191B-55ZMB
5962-8873402JA	WS57C191B-45YMB
5962-8873402LA	WS57C291B-45KMB
5962-88734023C	WS57C191B-45ZMB
5962-8766101XA	WS27C128F-90DMB
5962-8766101YC	WS27C128F-90CMB
5962-8766108XA	WS57C128F-70DMB
5962-8766108YC	WS57C128F-70CMB
5962-8873501KA	WS57C45-45HMB
5962-8873501LA	WS57C45-45KMB
5962-8873502KA	WS57C45-35HMB
5962-8873502LA	WS57C45-35KMB
5962-8873503KA	WS57C45-35HMB
5962-8873503LA	WS57C45-35KMB
5962-8961403XA	WS27C010L-20DMB
5962-8961403YC	WS27C010L-20CMB
5962-8961404XA	WS27C010L-17DMB
5962-8961404YC	WS27C010L-17CMB
5962-8961405XA	WS27C010L-15DMB
5962-8961405YC	WS27C010L-15CMB
5962-8961406XA	WS27C010L-12DMB
5962-8961406YC	WS27C010L-12CMB
8510204YA	WS27C64F-90DMB
8510204ZC	WS27C64F-90CMB
8510207YA	WS57C64F-70DMB
8510207ZC	WS57C64F-70CMB

Section Index

Programming/ Algorithms/ Erasure/ Programmers

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363.

PROGRAMMING/ERASURE/ PROGRAMMERS

PROGRAMMING

Upon delivery from WSI or after erasure, the EPROM has all bits in the "1" or high state. "0's" are loaded into the device through the procedure of programming.

Programming is performed by raising V_{CC} to its appropriate voltage (5.6 or 6.25 volts), disabling the outputs, raising V_{PP} to its appropriate programming voltage (12.5 to 13.5 Volts), enabling chip enable, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a programming pulse $\overline{PGM}$. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 μF and a 0.01 μF capacitor in parallel with V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

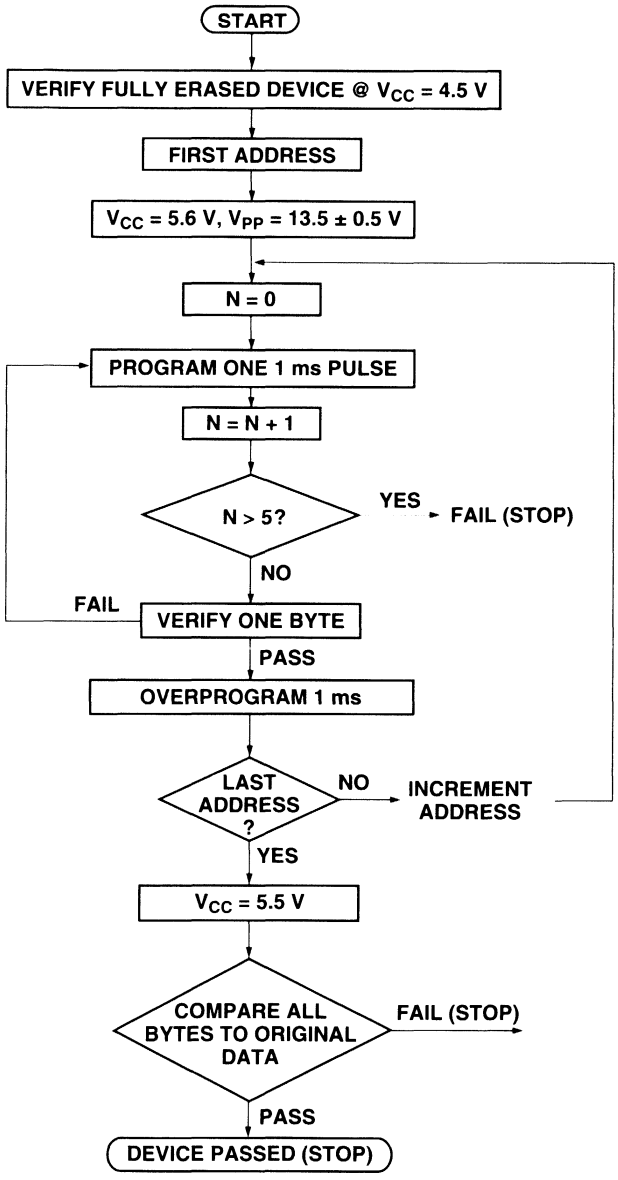
ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the EPROM to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 from 15 to 20 minutes. The EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

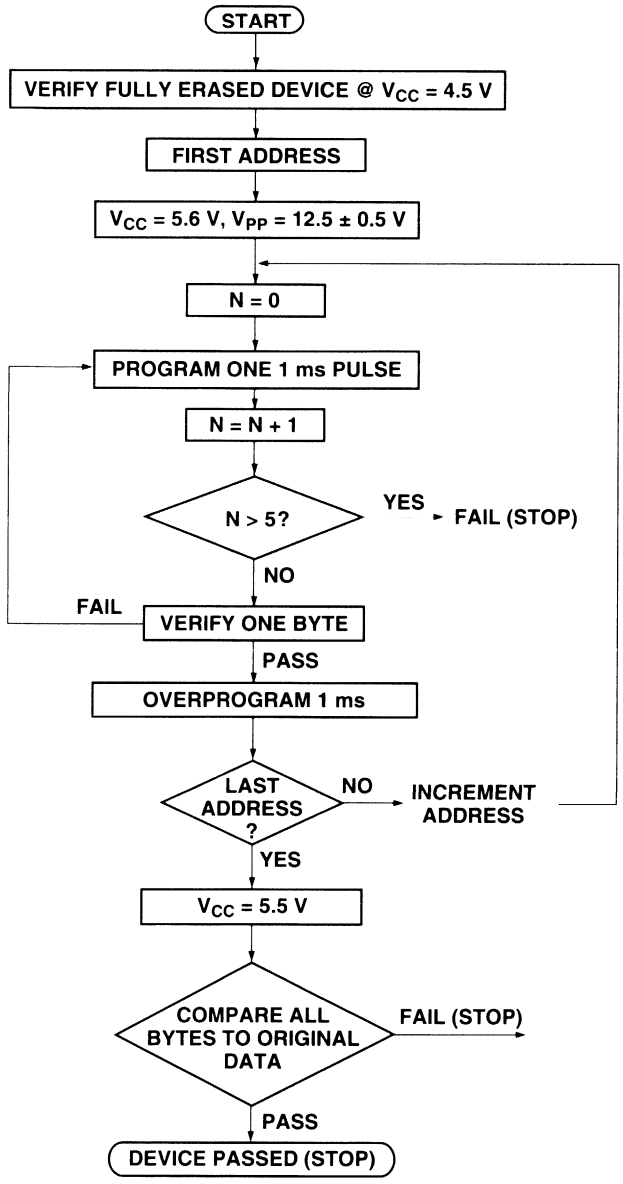
It is important to note that EPROMs and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase an EPROM and exposure to these light sources should be prevented to realize maximum system reliability. If used in such an environment, the EPROM package window should be covered by an opaque label or substance.

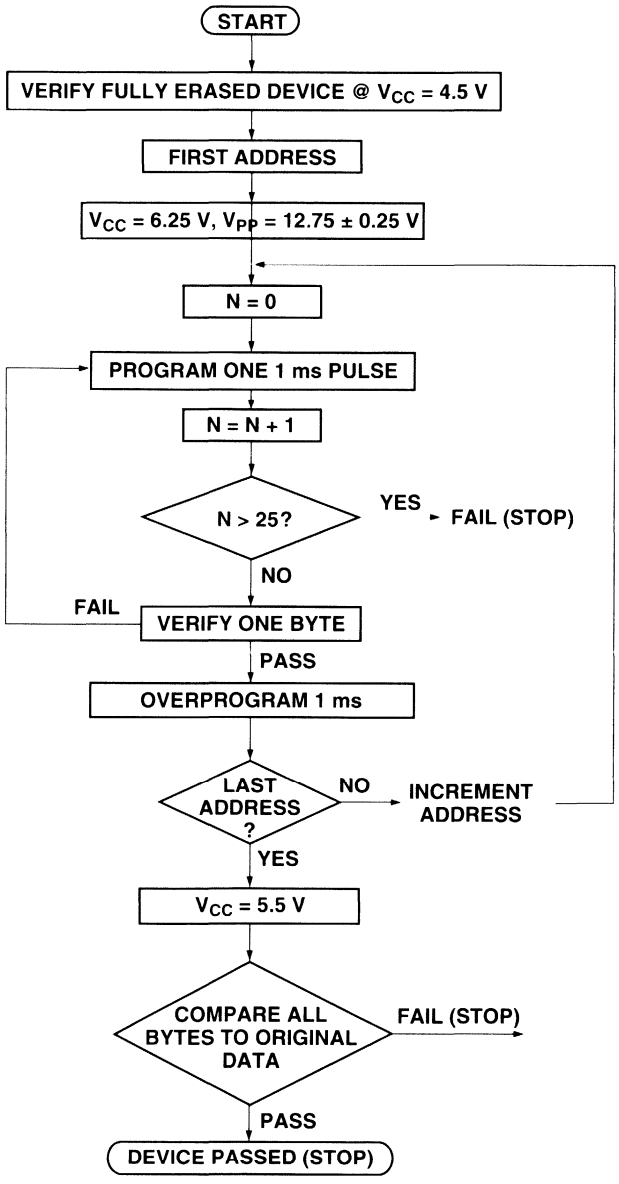
PROGRAMMERS

WSI's MagicPro™ IBM PC compatible engineering programmer and several commercially available engineering and production programmers support the WSI EPROM product family. A reference chart of Data I/O programmers follows.


START
VERIFY FULLY ERASED DEVICE @ V_{CC} = 4.5 V
FIRST ADDRESS
V_{CC} = 5.6 V, V_{PP} = 13.5 ± 0.5 V
N = 0
PROGRAM ONE 1 ms PULSE
N = N + 1
N > 5?
YES
FAIL (STOP)
NO
FAIL
VERIFY ONE BYTE
PASS
OVERPROGRAM 1 ms
LAST ADDRESS ?
NO
INCREMENT ADDRESS
YES
V_{CC} = 5.5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL (STOP)
PASS
DEVICE PASSED (STOP)

5


START
VERIFY FULLY ERASED DEVICE @ V_{CC} = 4.5 V
FIRST ADDRESS
V_{CC} = 5.6 V, V_{PP} = 12.5 ± 0.5 V
N = 0
PROGRAM ONE 1 ms PULSE
N = N + 1
N > 5?
YES
FAIL (STOP)
NO
FAIL
VERIFY ONE BYTE
PASS
OVERPROGRAM 1 ms
LAST ADDRESS ?
NO
INCREMENT ADDRESS
YES
V_{CC} = 5.5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL (STOP)
PASS
DEVICE PASSED (STOP)


START
VERIFY FULLY ERASED DEVICE @ V_{CC} = 4.5 V
FIRST ADDRESS
V_{CC} = 6.25 V, V_{PP} = 12.75 ± 0.25 V
N = 0
PROGRAM ONE 1 ms PULSE
N = N + 1
N > 25?
YES
FAIL (STOP)
NO
FAIL
VERIFY ONE BYTE
PASS
OVERPROGRAM 1 ms
LAST ADDRESS ?
NO
INCREMENT ADDRESS
YES
V_{CC} = 5.5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL (STOP)
PASS
DEVICE PASSED (STOP)

WS6000

MagicPro™ Memory and Programmable Peripheral Programmer

Key Features

- ❑ Programs All WSI CMOS Memory and and Programmable Peripheral Products and All Future Programmable Products
- ❑ Programs 24, 28, 32 and 40 Pin Standard 600 Mil or Slim 300 Mil Dip Packages without Adaptors
- ❑ Programs LCC, PGA and QFP Packaged Product by Using Adaptors
- ❑ Easy-to-Use Menu-Driven Software
- ❑ Compatible with IBM PC/XT/AT Family of Computers (and True Plug-Compatible

General Description

MagicPro is an engineering development tool designed to program existing WSI EPROMs, RPROMs, Programmable Peripherals, and future WSI programmable products. It is used within the IBM-PC® and compatible computers. The MagicPro is meant to bridge the gap betweeen the introduction of a new WSI programmable product and the availability of programming support from programmer manufacturers (e.g., Data I/O, etc.). The MagicPro programmer and accompanying software enable quick programming of newly released WSI programmable products, thus accelerating the system design process.

The MagicPro plug-in board is integrated easily into the IBM-PC. It occupies a short expansion slot and its software requires only 256K bytes of computer memory. The two external ZIF-Dip sockets in the Remote Socket Adaptor (RSA) support 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil Dip packages without adaptors. LCC, PGA and QFP packages are supported using adaptors.

Many features of the MagicPro Programmer show its capabilities in supporting WSI's future products. Some of these are:

- ❑ 24 to 40 pin JEDEC Dip Pinouts
- ❑ 1 Meg Address Space (20 address lines)
- ❑ 16 Data I/O Lines

General Description (Cont.)

The MagicPro menu driven software makes using different features of the MagicPro an easy task. Software updates are done via floppy disk which eliminates the need for adding a new memory device for system upgrading.

Please call 800-TEAM-WSI for information regarding programming WSI products not listed herein. The MagicPro reads Intel Hex format for use with assemblers and compilers.

MagicPro Commands

- ❑ Help
- ❑ Upload RAM from Device
- ❑ Load RAM from Disk
- ❑ Write RAM to Disk
- ❑ Display RAM Data
- ❑ Edit RAM
- ❑ Move/Copy RAM
- ❑ Fill RAM
- ❑ Blank Test Device
- ❑ Verify Device
- ❑ Program Device
- ❑ Select Device
- ❑ Configuration
- ❑ Quit MagicPro

Technical Information

- ❑ ***Size:***
  IBM-PC Short Length Card
- ❑ ***Port Address Location:***
  100H to 1FFH – default 140H (if a conflict exists with this address space, the address location can be changed in software and with the switches on the plug-in board.)
- ❑ ***System Memory Requirements:***
  256K Bytes of RAM
- ❑ ***Power:***
  + 5 Volts, 0.03 Amp; +12 Volts, 0.04 Amp
- ❑ ***Remote Socket Adaptor (RSA):***
  The RSA contains two ZIF-Dip sockets that are used to program and read WSI programmable products. The 32 pin ZIF-Dip socket supports 24, 28 and 32 pin standard 600 mil or slim 300 mil Dip packaged product. The 40 pin ZIF-Dip socket supports all 40 pin Dip packages. Adaptor sockets are available for LCC, PGA and QFP packages.

Ordering Information

The WS6000 MagicPro Systems Contains:

- ❑ MagicPro IBM-PC Plug-in Programmer Board
- ❑ MagicPro Remote Socket Adaptor and Cable
- ❑ MagicPro Operating System Floppy Disk and Operating Manual

The WS6000 MagicPro Adaptors Include:

- ❑ WS6001 28-Pin CLLCC Package Adaptor for Memory.
- ❑ WS6008 28-Pin 0.3" Wide Dip Adaptor for SAM448
- ❑ WS6009 28-Pin PLDCC/CLDCC/ CLLCC Package Adaptor for SAM448
- ❑ WS6010 88-Pin PGA Package Adaptor for PAC1000
- ❑ WS6012 32-Pin CLDCC Package Adaptor for Memory
- ❑ WS6015 44-Pin PGA Package Adaptor for MAP168 and PSD3XX
- ❑ WS6020 52-Pin PQFP Package Adaptor for PSD3XX
- ❑ WS6021 44-Pin CLDCC/PLDCC Package Adaptor for PSD3XX

DATA I/O PROGRAMMING SUPPORT

(Software Versions)

		Current Revision.		*3.8*	*3.8*	*3.8*	*3.8*	*3.8*	*1.9*	*1.3*	*1*	*25*
		WSI		Unisite	Unisite	Unisite	Unisite	Unisite			3900	
	Device	Package	Package	Pins	40	48	Chipsite	Pinsite	Setsite	2900	3900	Autosite	S1000
High-Performance CMOS PROMs and RPROMs													
	57C43B	DIP	D,T,S	24	2.5	2.5			2.5	1.3	1	1	20
		FP	F	24									
		LCC	C	28			2.5	3		1.3	1	1	
		LDCC	J	28			2.5	3		1.3	1	1	
	57C43C	DIP	D,S,T	24	3.8	3.8				1.9	1.3	1	25
		FP	F	24									
		LCC	C	28			3.8	3.8		1.9	1.3		
		LDCC	J	28			3.8	3.8		1.9	1.3		
	57C45	DIP	K,S,T	24	2.7	2.7				1.2	1	1	
		FP	F	24									
		LCC	C,Z	28			3.7	3.7		1.8	1		
	57C49B	DIP	D,P,S,T	24	2.5	2.5			2.8	1.3	1	1	20
		FP	F	24									
		LCC	C	28			2.5	3		1.3	1		
		LDCC	J	28			2.5	3		1.3	1		
	57C49C	DIP	D,P,S,T	24	3.7	3.7				1.8	1.2	1	25
		FP	F	24									
		LCC	C	28			3.8	3.8		1.9	1.3		
		LDCC	J	28			3.8	3.8		1.9	1.3		
	57C51B	DIP	D,T	28	2.5	2.5			3	1.3	1	1	20
		LCC	C	32			2.5	3		1.3	1		
		LDCC	J,L	32			2.5	3		1.3	1		
	57C51C	DIP	D,T	28	3.4	3.4			3.9*	1.5	1	1	25
		LCC	C	32			3.8	3.8		1.9	1.3		
		LDCC	J,L	32			3.8	3.8		1.9	1.3		
	57C71C	DIP	D,T	28	3	3				1.3	1	1	
		LCC	C	32									
		LDCC	J,L	32									
	57C191B	DIP	D,P,Y	24	2.5	2.5			2.8	1.3	1		20
		FP	F	24									
		LCC	C,Z	28			2.5	3		1.3	1	1	
		LDCC	J	28			2.5	3		1.3	1	1	
	57C291B	DIP	K,S,T	24	2.5	2.5				1.5	1	1	
	57C191C	DIP	D,P,Y	24	2.5	2.5				1.3	1	1	20
		FP	F	24									
		LCC	C,Z	28									
		LDCC	J	28									
	57C291C	DIP	K,S,T	24	2.5	2.5				1.5	1	1	
	LCC - Leadless Chip Carrier												
	LDCC - Leaded Chip Carrier												
	FP - Flat Pack												
	*Planned for the next release from DATA I/O												

5

DATA I/O PROGRAMMING SUPPORT

(Software Versions)

All WSI memory products program easily on standard commercially available EPROM programmers. Manufacturers of these EPROM programmers offer a broad range of products which cover prototyping through high volume production requirements. The table below covers that portion of Data I/O's and WSI's product line which supports WSI's programmable products.

MagicPro™ PROGRAMMING SUPPORT

WSI's MagicPro programmer programs all WSI RPROM and EPROM memories. More details on the MagicPro programmer are found on page 5-9 of this section.

For more information regarding programming support for WSI products call toll-free 800-TEAM WSI (800-832-6974) or 800-451-5970 (CA).

	Current Revision.			3.8	3.8	3.8	3.8	3.8	1.9	1.3	1	25
		WSI		Unisite	Unisite	Unisite	Unisite	Unisite			3900	
Device	Package	Package	Pins	40	48	Chipsite	Pinsite	Setsite	2900	3900	Autosite	S1000
High-Performance CMOS EPROMs												
27C64F	DIP	D	28	2	2			2	1	1	1	7
	LCC	C	32									
57C64F	DIP	D	28	2	2			2	1.3	1	1	1
	LCC	C	32			2.4	3		1.3	1		
	LDCC	J	32			2.4	3		1.3	1		
27C128F	DIP	D	28	2	2			2	1	1	1	7
	LCC	C	32			2.4	3		1.2	1		
57C128F	DIP	D	28	2.5	2.5			2.8	1.3	1	1	1
	LCC	C	32			3.8	3.8		1.9	1.3		
57C128FB	DIP	D	28	3.9*	3.9*			3.9*	2.0*	1.4*		24
	LCC	C	32			3.9*	3.9*		2.0*	1.4*		24
	LDCC	L,J	32			3.9*	3.9*		2.0*	1.4*		24
27C256F	DIP	D	28	2.4	2.4			3	1	1	1	23
	LCC	C	32			2.4	3		1.2	1		
	LDCC	L	32			2.4	3		1.2	1		
57C256F	DIP	D,P,T	28	2.4	2.4				1.3	1	1	22
	LCC	C	32			2.4	3		1.5	1		
	LDCC	J,L	32			2.4	3		1.5	1		
57C256FB	DIP	D,P,T	28	3.9*	3.9*				2.0*	1.4*		26*
	LCC	C	32			3.9*	3.9*		2.0*	1.4*		26*
	LDCC	L,J	32			3.9*	3.9*		2.0*	1.4*		26*
LCC - Leadless Chip Carrier												
LDCC - Leaded Chip Carrier												
FP - Flat Pack												
*Planned for the next release from DATA I/O												

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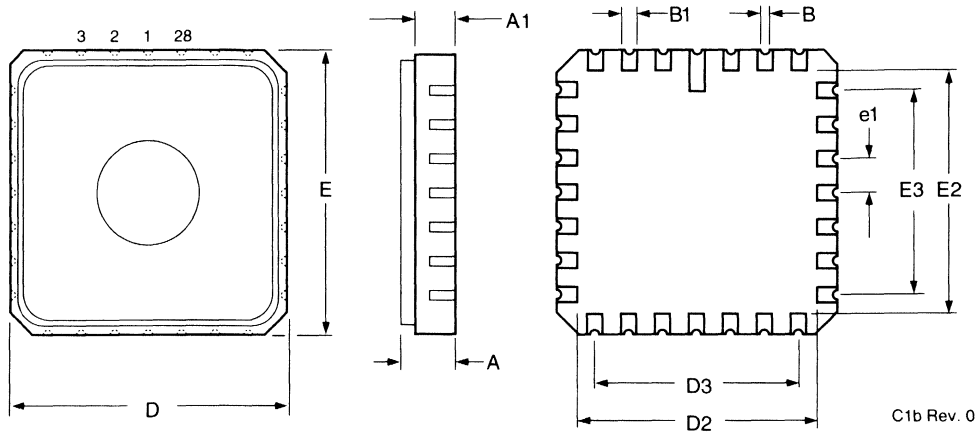
Section Index

Package Information

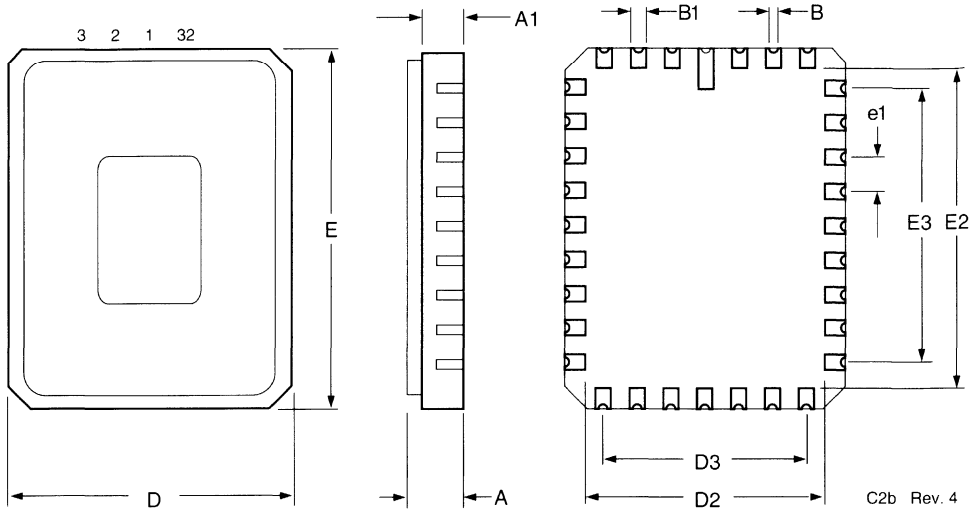
DRAWING C1 28 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



Family: Ceramic Leadless Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.41	3.30		0.095	0.130	
A1	1.37	1.96		0.054	0.077	
B	0.46		Typical Dia.	0.018		Typical Dia.
B1	0.56	0.71		0.022	0.028	
D	11.23	11.68		0.442	0.460	
D2	8.89		Typical	0.350		Typical
D3	7.62		Reference	0.300		Reference
E	11.23	11.68		0.442	0.460	
E2	8.89		Typical	0.350		Typical
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
N	28			28		

C1b

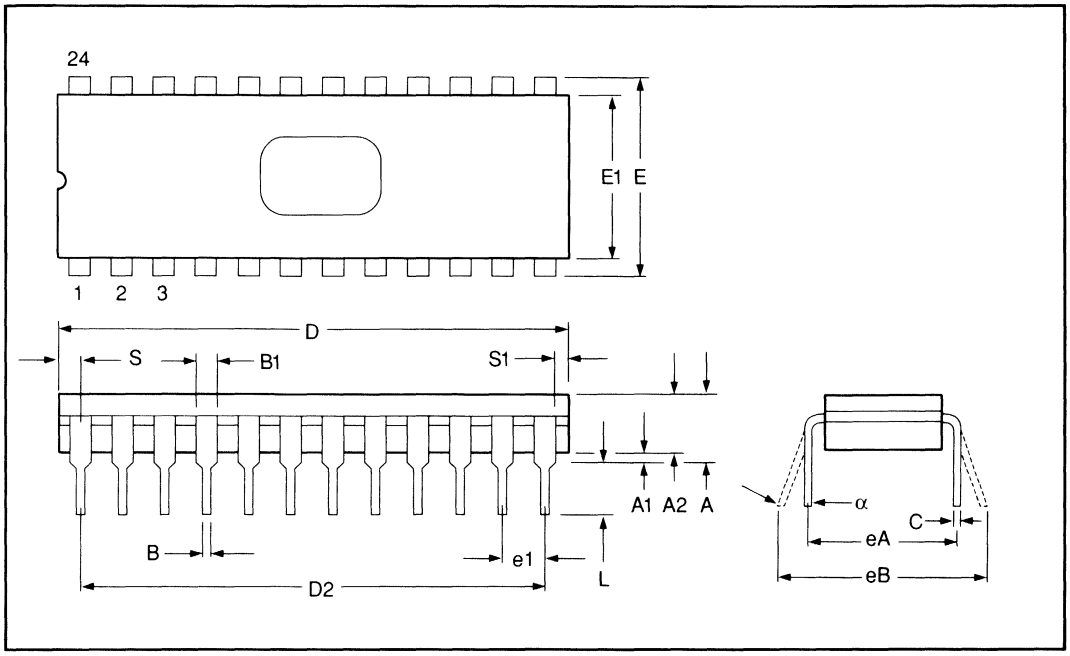
DRAWING C2 32 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



Family: Ceramic Leadless Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.41	3.05		0.095	0.120	
A1	1.27	2.03		0.050	0.080	
B	0.46		Typical Dia.	0.018		Typical Dia.
B1	0.56	0.71		0.022	0.028	
D	11.23	11.63		0.442	0.458	
D2	8.89		Typical	0.350		Typical
D3	7.62		Reference	0.300		Reference
E	13.72	14.22		0.540	0.560	
E2	11.43		Typical	0.450		Typical
E3	10.16		Reference	0.400		Reference
e1	1.27		Reference	0.050		Reference
N	32			32		

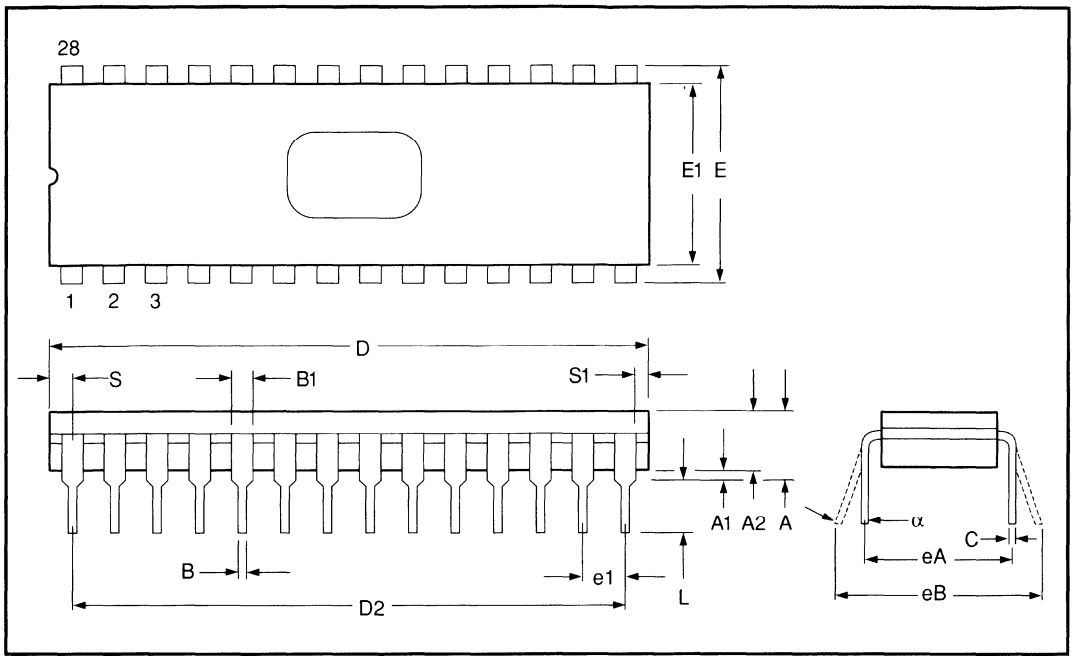
C2B

DRAWING D1 24 Pin CERDIP (Package Type D)



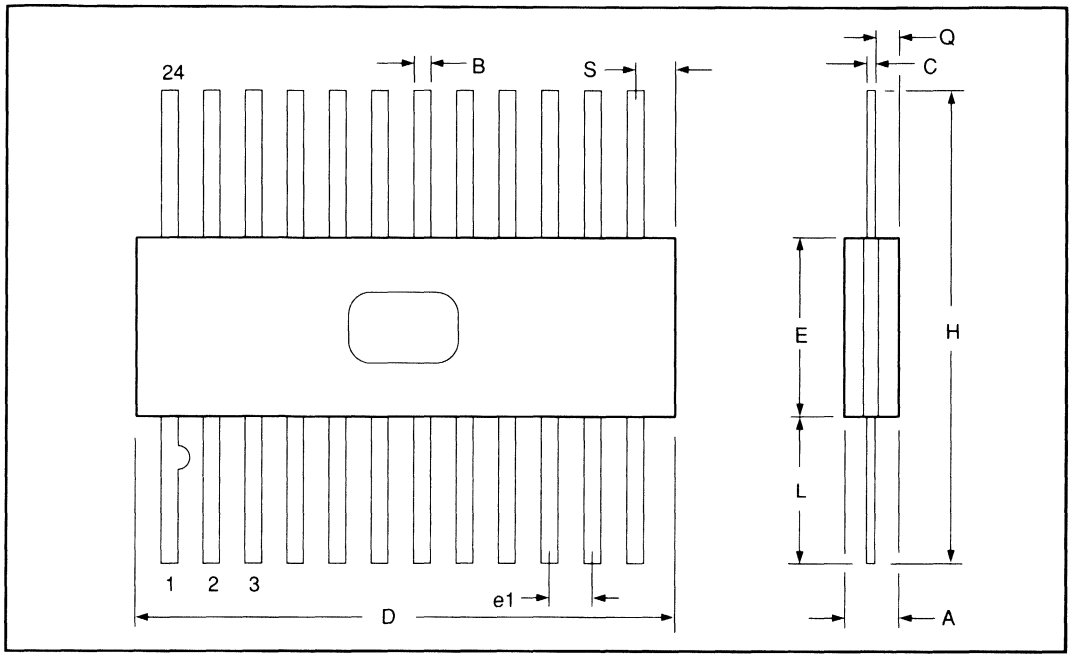
Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.81	5.72		0.150	0.225	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	31.50	32.77		1.240	1.290	
D2	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E1	13.08	15.37		0.515	0.605	
e1	2.54		Reference	0.100		Reference
eA	15.49		Reference	0.610		Reference
eB	15.75	17.78		0.620	0.700	
L	3.18	4.70		0.125	0.185	
N	24		600 MIL	24		600 MIL
S	1.40	2.29		0.055	0.090	
S1	0.25	-		0.010	-	

DRAWING D2 28 Pin CERDIP (Package Type D)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.81	5.72		0.150	0.225	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	36.58	37.85		1.440	1.490	
D2	33.02		Reference	1.300		Reference
E	15.24	15.75		0.600	0.620	
E1	13.08	15.37		0.515	0.605	
e1	2.54		Reference	0.100		Reference
eA	15.49		Reference	0.610		Reference
eB	15.75	17.78		0.620	0.700	
L	3.18	4.70		0.125	0.185	
N	28		600 MIL	28		600 MIL
S	1.40	2.29		0.055	0.090	
S1	0.25	-		0.010	-	

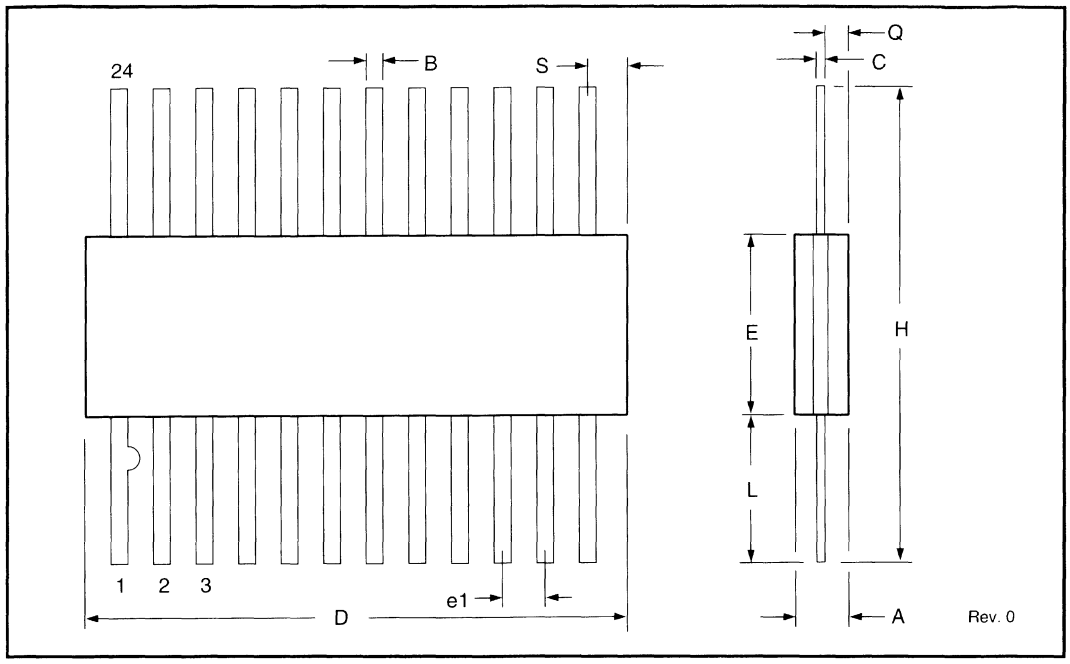
DRAWING F1 24 Pin Ceramic Flatpack (Package Type F)



Family: Ceramic Flatpack						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.52	2.29		0.060	0.090	
B	0.38	0.48		0.015	0.019	
C	0.08	0.15		0.003	0.006	
D	14.73	16.26		0.580	0.640	
E	8.64	10.67		0.340	0.420	
e1	1.27		Reference	0.050		Reference
H	22.86	25.40		0.900	1.000	
L	6.35	8.89		0.250	0.350	
N	24			24		
Q	0.66	1.14		0.026	0.045	
S	-	1.14		-	0.045	

F1

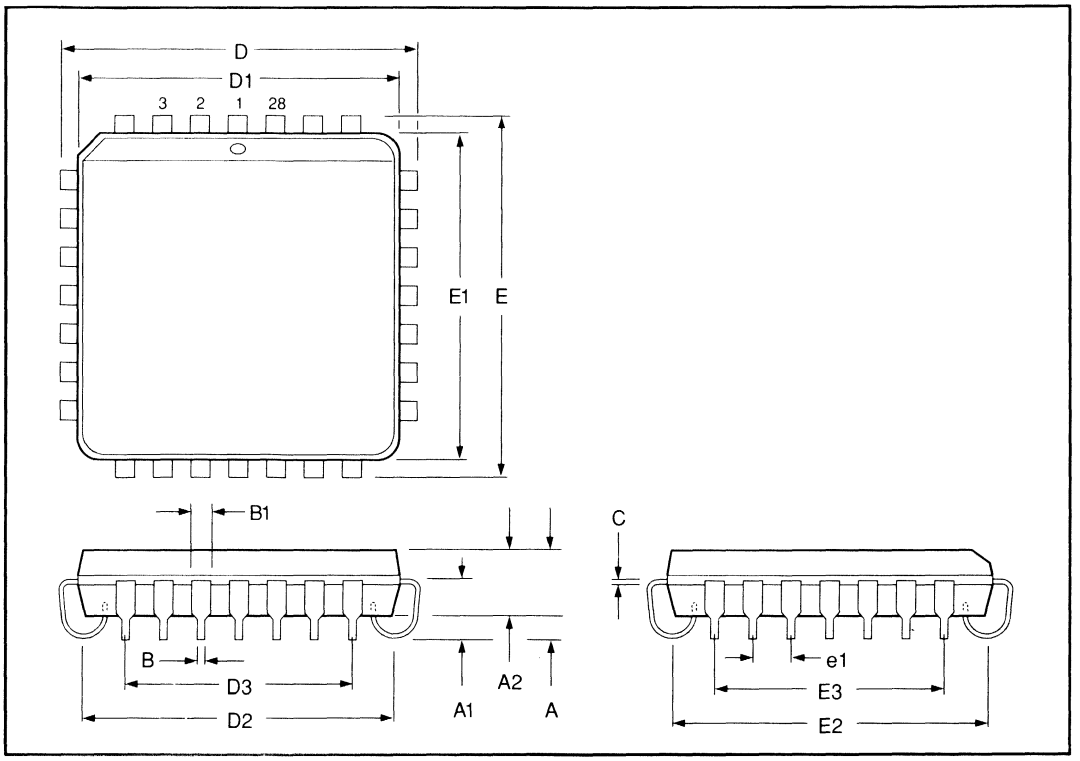
DRAWING H1 24 Pin Ceramic Flatpack (Package Type H)



Family: Ceramic Flatpack						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.52	2.29		0.060	0.090	
B	0.38	0.48		0.015	0.019	
C	0.08	0.15		0.003	0.006	
D	14.73	16.26		0.580	0.640	
E	8.64	10.67		0.340	0.420	
e1	1.27		Reference	0.050		Reference
H	22.86	25.40		0.900	1.000	
L	6.35	8.89		0.250	0.350	
N	24			24		
Q	0.66	1.14		0.026	0.045	
S	-	1.14		-	0.045	

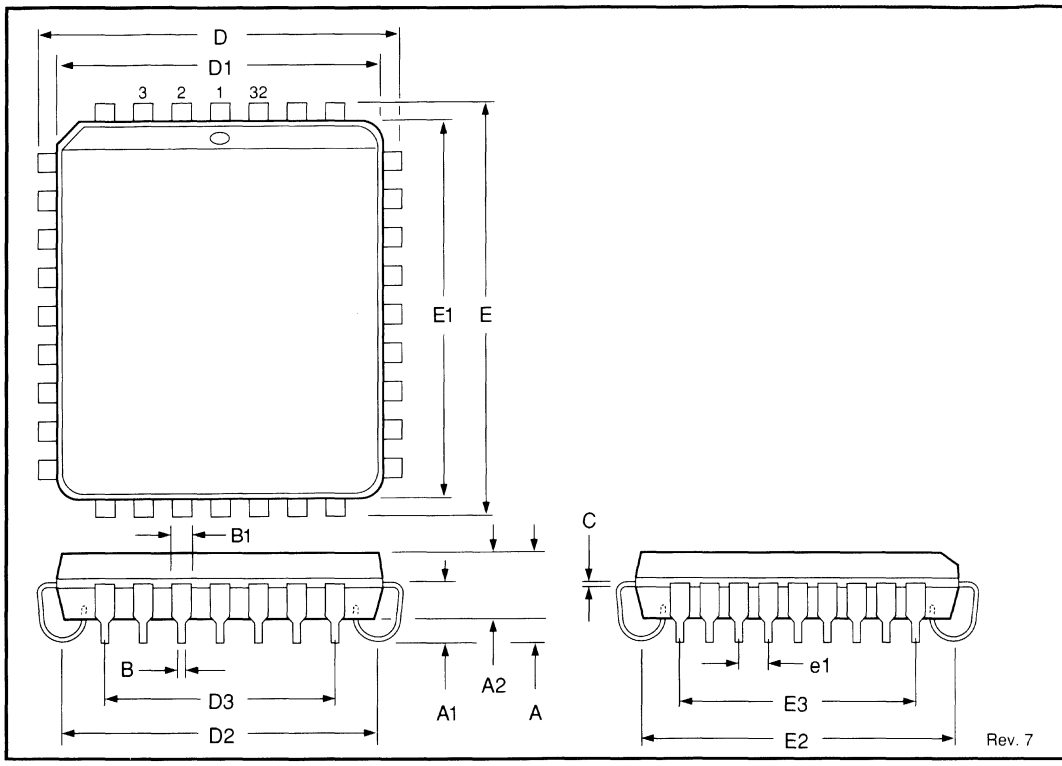
H1

DRAWING J3 28 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



Family: Plastic Leaded Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.76	3.96		0.148	0.156	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	12.32	12.57		0.485	0.495	
D1	11.43	11.53		0.450	0.454	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	12.32	12.57		0.485	0.495	
E1	11.43	11.53		0.450	0.454	
E2	9.91	10.92		0.390	0.430	
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
N	28			28		

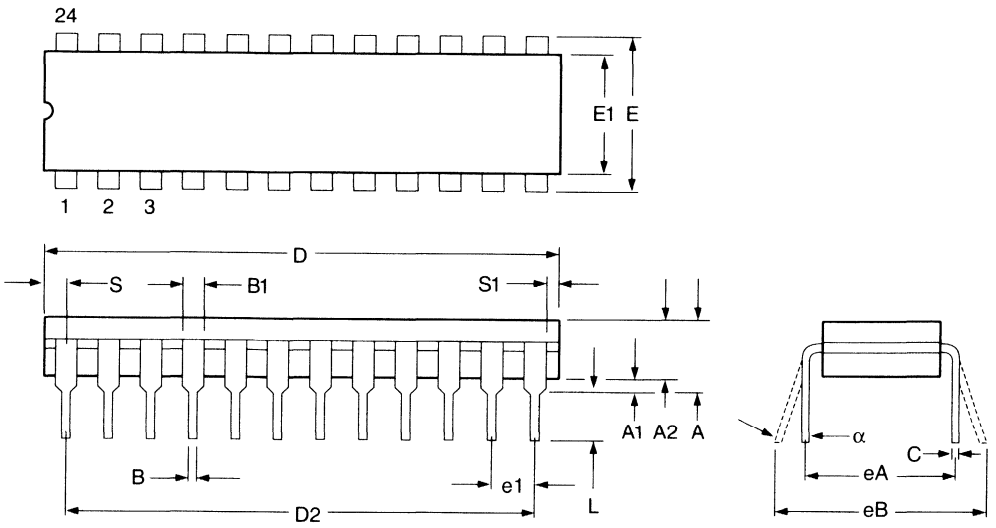
DRAWING J4 32 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



Family: Plastic Leaded Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.12	3.56		0.123	0.140	
A1	1.98	2.41		0.078	0.095	
A2	2.69	2.84		0.106	0.112	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	12.32	12.57		0.485	0.495	
D1	11.40	11.51		0.449	0.453	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	14.86	15.11		0.585	0.595	
E1	13.94	14.05		0.549	0.553	
E2	12.45	13.46		0.490	0.530	
E3	10.16		Reference	0.400		Reference
e1	1.27		Reference	0.050		Reference
N	32			32		

J4

DRAWING K1 24 Pin CERDIP (Package Type K)

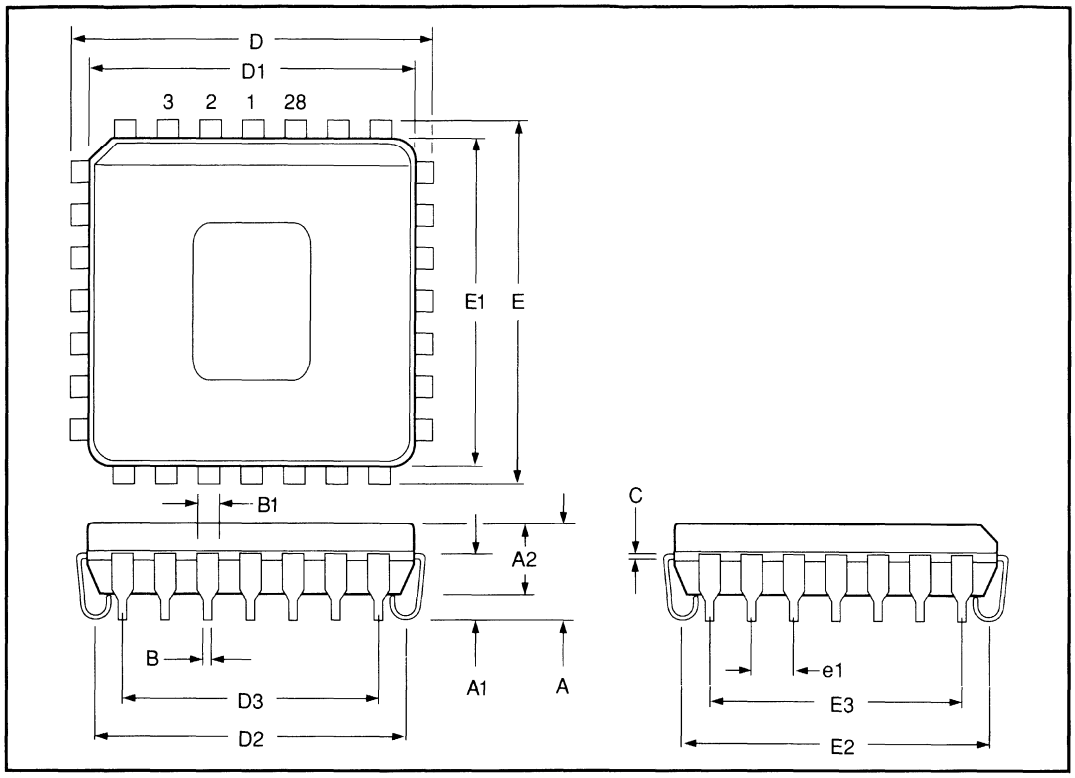


Rev. 6

Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.68	5.08		0.145	0.200	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.41	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	31.50	32.51		1.240	1.280	
D2	27.94		Reference	0.100		Reference
E	7.62	8.13		0.300	0.320	
E1	7.11	7.87		0.280	0.310	
e1	2.54		Reference	0.100		Reference
eA	7.87		Reference	0.310		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	4.70		0.125	0.185	
N	24		300 MIL	24		300 MIL
S	1.40	2.29		0.055	0.090	
S1	0.13	-		0.005	-	

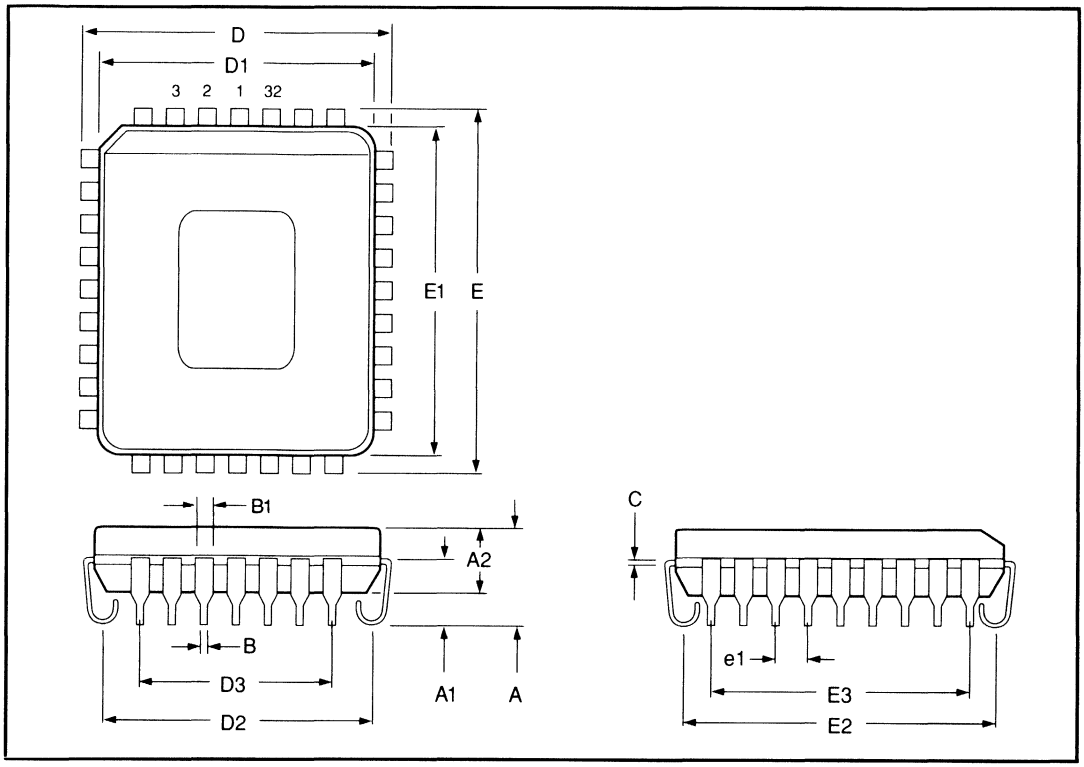
K1

DRAWING L2 28 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



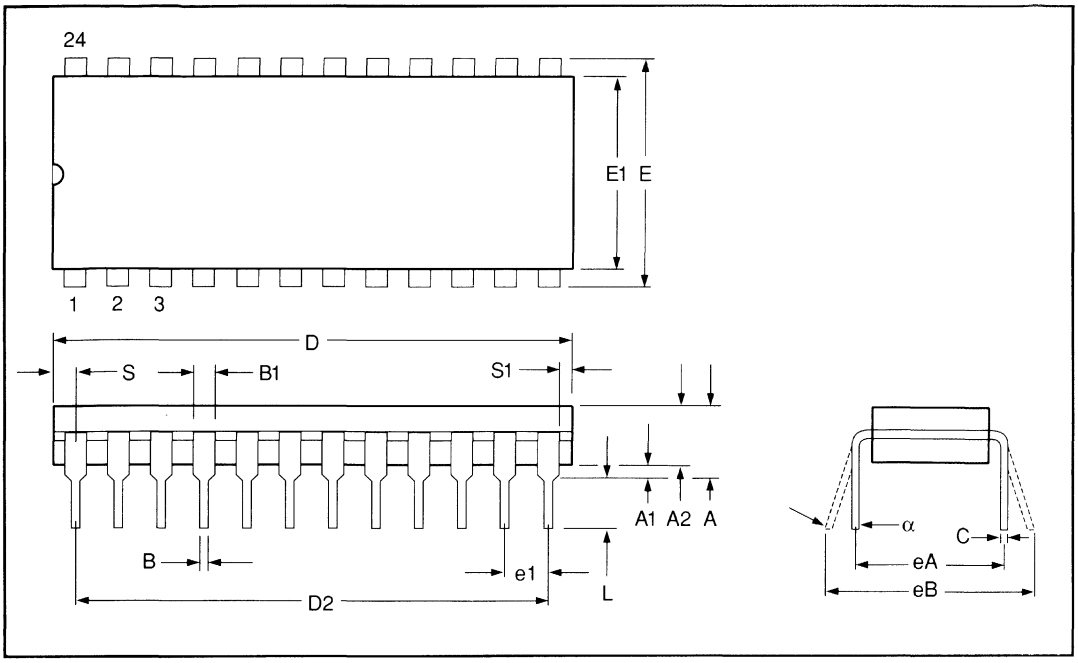
Family: Ceramic Leaded Chip Carrier-CERQUAD						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.94	4.57		0.155	0.180	
A1	2.29	2.92		0.090	0.115	
A2	3.05	3.68		0.120	0.145	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15	0.25		0.006	0.010	
D	12.06	12.57		0.475	0.495	
D1	10.92	11.56		0.430	0.455	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	12.06	12.57		0.475	0.495	
E1	10.92	11.56		0.430	0.455	
E2	9.91	10.92		0.390	0.430	
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
N	28			28		

DRAWING L3 32 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



Family: Ceramic Leaded Chip Carrier-CERQUAD						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.30	4.06		0.130	0.160	
A1	1.91	2.29		0.075	0.090	
A2	2.29	3.05		0.090	0.120	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15		Typical	0.006		Typical
D	12.32	12.57		0.485	0.495	
D1	10.92	11.56		0.430	0.455	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	14.86	15.11		0.585	0.595	
E1	13.77	14.12		0.542	0.556	
E2	12.95	13.46		0.510	0.530	
E3	10.16		Reference	0.400		Reference
e1	1.27		Reference	0.050		Reference
N	32			32		

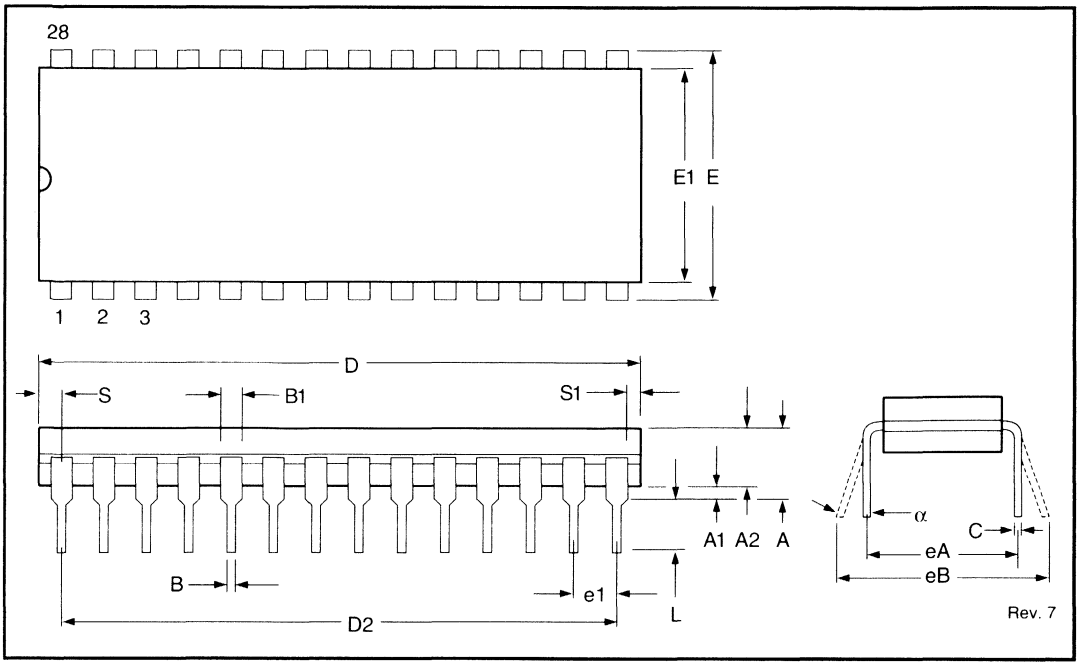
DRAWING P2 24 Pin Plastic DIP (Package Type P)



Family: Plastic Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	-	4.83		-	0.190	
A1	0.38	-		0.015	-	
A2	3.81		Typical	0.150		Typical
B	0.38	0.56		0.015	0.022	
B1	1.40	1.65		0.055	0.065	
C	0.20	0.30		0.008	0.012	
D	31.62	31.88		1.245	1.255	
D2	27.94		Reference	1.100		Reference
E	15.24	15.88		0.600	0.625	
E1	13.46	14.22		0.530	0.560	
e1	2.54		Reference	0.100		Reference
eA	15.24		Reference	0.600		Reference
eB	15.24	17.78		0.600	0.700	
L	3.18	3.43		0.125	0.135	
N	24		600 Mil	24		600 Mil
S	1.78	2.03		0.070	0.080	
S1	0.76	-		0.030	-	

P2

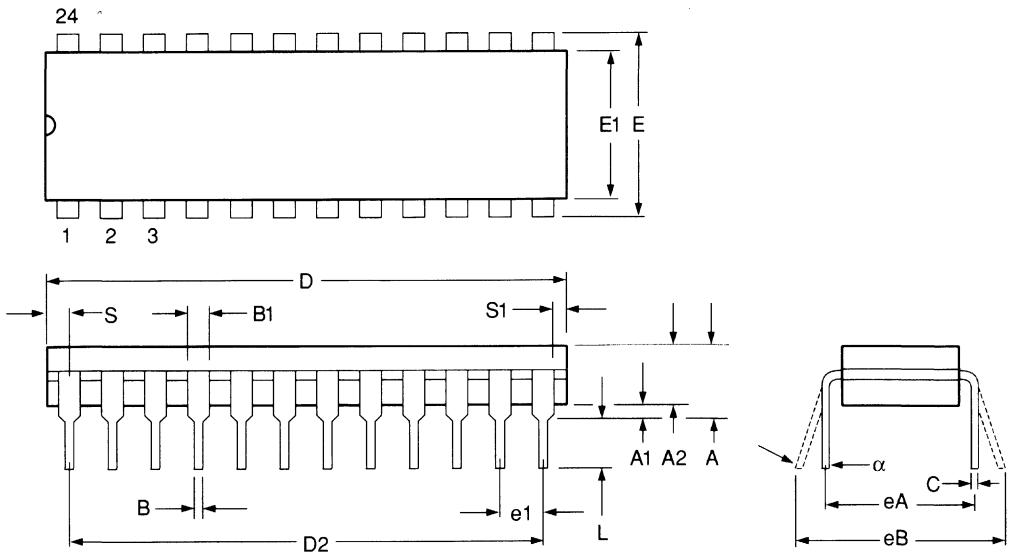
DRAWING P3 28 Pin Plastic DIP (Package Type P)



Family: Plastic Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	-	4.83		-	0.190	
A1	0.38	-		0.015	-	
A2	3.81		Typical	0.150		Typical
B	0.38	0.56		0.015	0.022	
B1	1.40	1.65		0.055	0.065	
C	0.20	0.30		0.008	0.012	
D	36.70	36.96		1.445	1.455	
D2	33.02		Reference	1.300		Reference
E	15.24	15.88		0.600	0.625	
E1	13.46	14.22		0.530	0.560	
e1	2.54		Reference	0.100		Reference
eA	15.24		Reference	0.600		Reference
eB	15.24	17.78		0.600	0.700	
L	3.18	3.43		0.125	0.135	
N	28		600 Mil	28		600 Mil
S	1.78	2.03		0.070	0.080	
S1	0.76	-		0.030	-	

P3

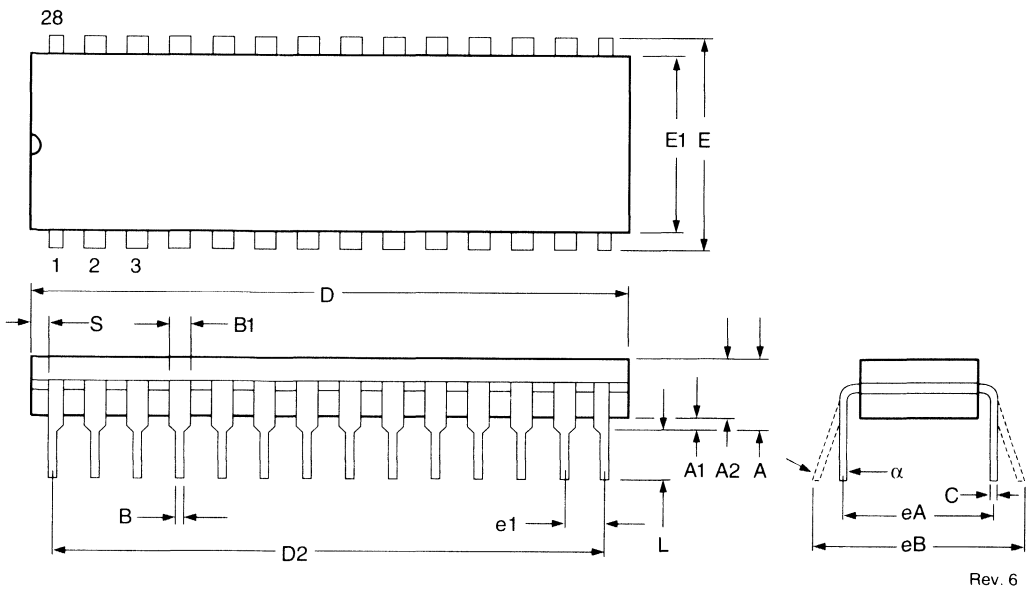
DRAWING S1 24 Pin Plastic .300 DIP (Package Type S)



	Millimeters			Inches		
Symbol	**Min**	**Max**	**Notes**	**Min**	**Max**	**Notes**
α	0°	15°		0°	15°	
A	-	4.32		-	0.170	
A1	0.38	-		0.015	-	
A2	3.56		Typical	0.140		Typical
B	0.38	0.56		0.015	0.022	
B1	1.40	1.65		0.055	0.065	
C	0.20	0.30		0.008	0.012	
D	31.88	31.13		1.255	1.265	
D2	27.94		Reference	1.100		Reference
E	7.62	8.26		0.300	0.325	
E1	6.35	6.86		0.250	0.270	
e1	2.54		Reference	0.100		Reference
eA	7.62		Reference	0.300		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	3.43		0.125	0.135	
N	24		300 Mil	24		300 Mil
S	1.78	2.16		0.070	0.085	

S1

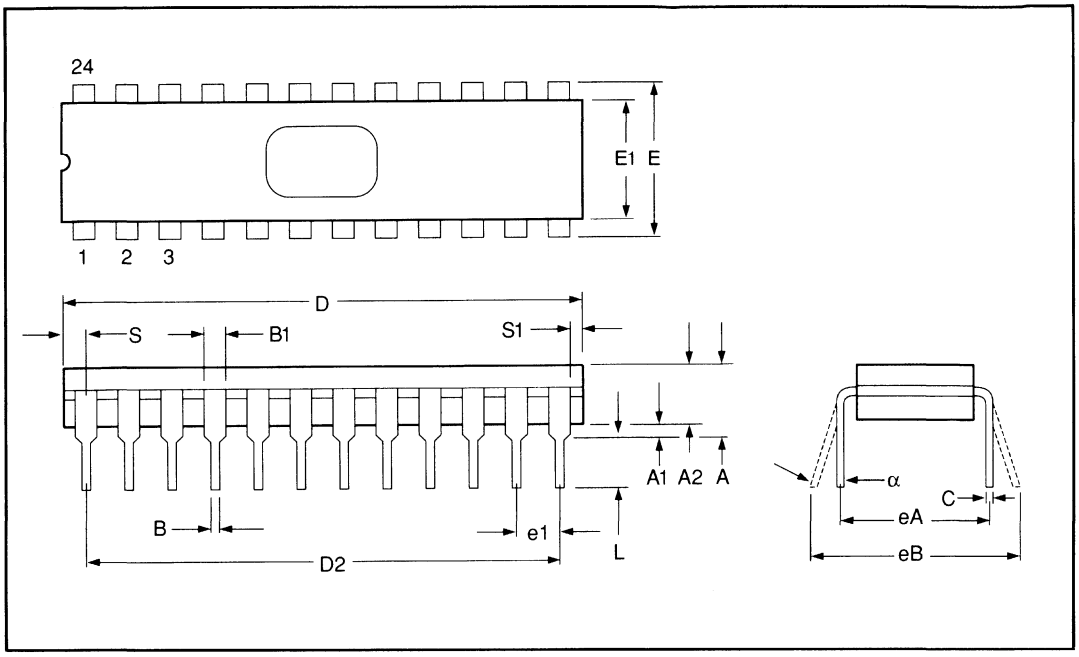
DRAWING S2 28 Pin Plastic .300 DIP (Package Type S)



Family: Plastic Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	-	4.32		-	0.170	
A1	0.38	-		0.015	-	
A2	3.56		Typical	0.140		Typical
B	0.38	0.56		0.015	0.022	
B1	1.02	1.40		0.040	0.055	
C	0.20	0.30		0.008	0.012	
D	34.16	35.31		1.345	1.390	
D2	33.02		Reference	1.300		Reference
E	7.62	8.26		0.300	0.325	
E1	6.86	7.37		0.270	0.290	
e1	2.54		Reference	0.100		Reference
eA	7.62		Reference	0.300		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	3.43		0.125	0.135	
N	28		300 Mil	28		300 Mil
S	0.51	1.17		0.020	0.046	

S2

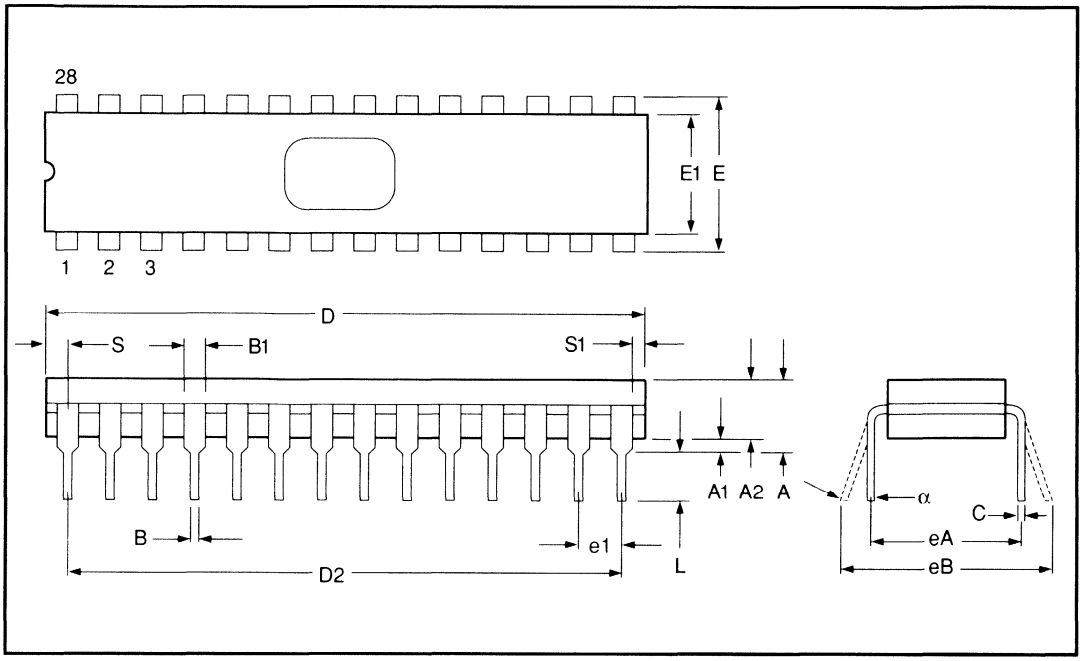
DRAWING T1 24 Pin CERDIP (Package Type T)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
a	0°	15°		0°	15°	
A	3.68	5.08		0.145	0.200	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.41	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	31.50	32.51		1.240	1.280	
D2	27.94		Reference	1.100		Reference
E	7.62	8.13		0.300	0.320	
E1	7.11	7.87		0.280	0.310	
e1	2.54		Reference	0.100		Reference
eA	7.87		Reference	0.310		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	4.70		0.125	0.185	
N	24		300 MIL	24		300 MIL
S	1.40	2.29		0.055	0.090	
S1	0.13	-		0.005	-	

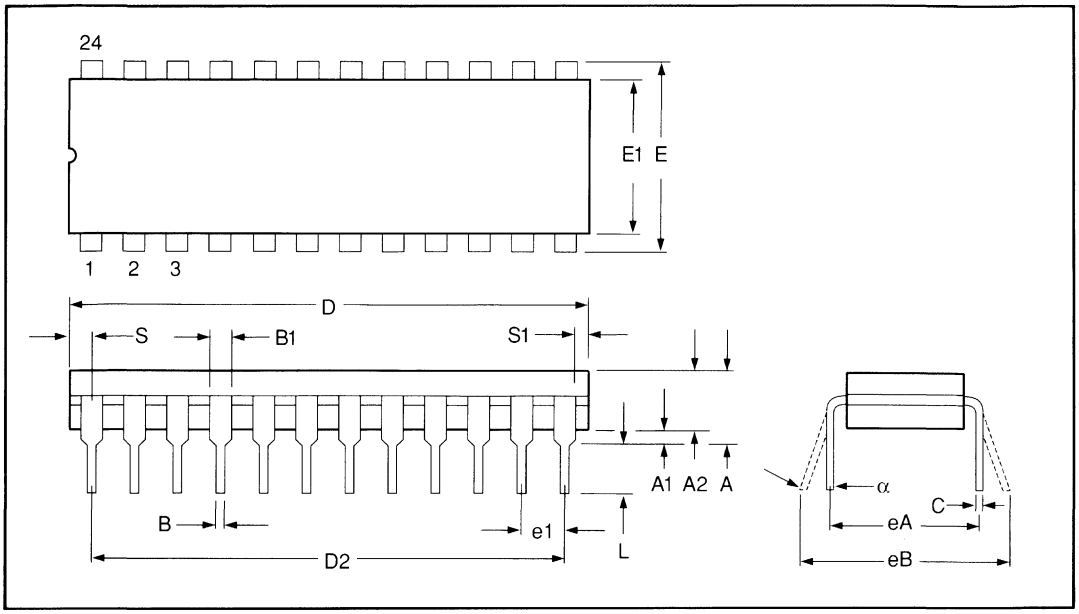
t1

DRAWING T2 28 Pin CERDIP (Package Type T)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.68	5.08		0.145	0.200	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	36.58	37.59		1.440	1.480	
D2	33.02		Reference	1.300		Reference
E	7.62	8.13		0.300	0.320	
E1	7.11	7.87		0.280	0.310	
e1	2.54		Reference	0.100		Reference
eA	7.87		Reference	0.310		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	4.70		0.125	0.185	
N	28		300 MIL	28		300 MIL
S	1.40	2.29		0.055	0.090	
S1	0.13	-		0.005	-	

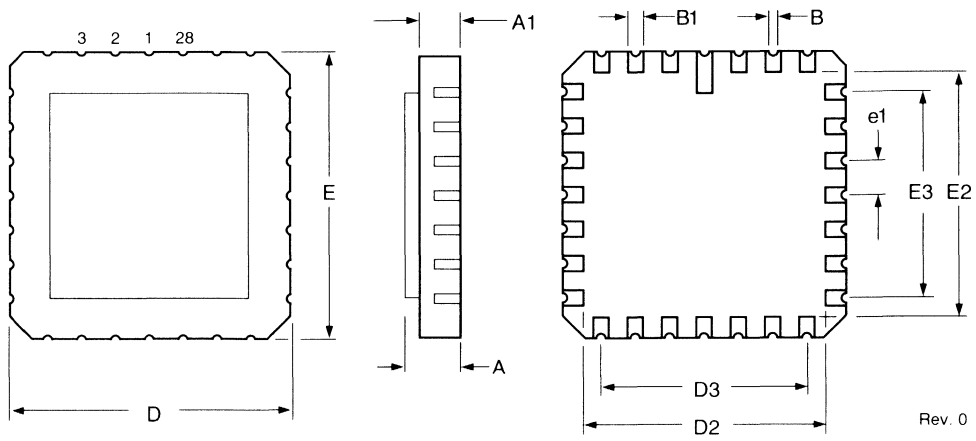
DRAWING Y3 24 Pin CERDIP (Package Type Y)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.81	5.72		0.150	0.225	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	31.50	32.77		1.240	1.290	
D2	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E1	13.08	15.37		0.515	0.605	
e1	2.54		Reference	0.100		Reference
eA	15.49		Reference	0.610		Reference
eB	15.75	17.78		0.620	0.700	
L	3.18	4.70		0.125	0.185	
N	24		600 MIL	24		600 MIL
S	1.40	2.29		0.055	0.090	
S1	0.25	-		0.010	-	

Y3

DRAWING Z2 28 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type Z)



Family: Ceramic Leadless Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.90	2.54		0.075	0.100	
A1	1.52	1.96		0.060	0.077	
B	0.41		Typical Dia.	0.016		Typical Dia.
B1	0.56	0.71		0.022	0.028	
D	11.23	11.68		0.442	0.460	
D2	8.89		Typical	0.350		Typical
D3	7.62		Reference	0.300		Reference
E	11.30	11.68		0.442	0.460	
E2	8.89		Typical	0.350		Typical
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
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Sales Representatives and Distributors

For additional information,
Call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363

Sales Representatives and Distributors

Domestic Representatives

ALABAMA

Rep. Inc.
Huntsville
Tel: (205) 881-9270
Fax: (205) 882-6692

ARIZONA

Summit Sales
Scottsdale
Tel: (602) 998-4850
Fax: (602) 998-5274

CALIFORNIA

Bager Electronics, Inc.
Fountain Valley
Tel: (714) 957-3367
Fax: (714) 546-2654

Bager Electronics, Inc.
Woodland Hills
Tel: (818) 712-0011
Fax: (818) 712-0160

Earle Assoc., Inc.
San Diego
Tel: (619) 278-5441
Fax: (619) 278-5443

I Squared, Inc.
Santa Clara
Tel: (408) 988-3400
Fax: (408) 988-2079

CANADA

Intelatech, Inc.
Mississauga
Tel: (416) 629-0082
Fax: (416) 629-1795

COLORADO

Waugaman Associates, Inc.
Wheat Ridge
Tel: (303) 423-1020
Fax: (303) 467-3095

CONNECTICUT

Advanced Tech Sales
Wallingford
Tel: (203) 284-0838
Fax: (203) 284-8232

FLORIDA

QXi of Florida, Inc.
Fort Lauderdale
Tel: (305) 978-0120
Fax: (305) 972-1408

QXi of Florida, Inc.
Orlando
Tel: (407) 872-2321
Fax: (407) 321-2098

QXi of Florida, Inc.
St. Petersburg
Tel: (813) 894-4556
Fax: (813) 894-3989

GEORGIA

Rep. Inc.
Tucker
Tel: (404) 938-4358
Tax: (404) 938-0194

ILLINOIS

Victory Sales
Hoffman Estates
Tel: (708) 490-0300
Telex: 206248
Fax: (708) 490-1499

INDIANA

Giesting & Associates
Carmel
Tel: (317) 844-5222
Fax: (317) 844-5861

IOWA

Gassner & Clark Co.
Cedar Rapids
Tel: (319) 393-5763
Twx: 62950087
Fax: (319) 393-5799

KANSAS/NEBRASKA

C. Logsdon & Assoc.
Prairie Village
Tel: (913) 381-3833
Fax: (913) 381-9774

KENTUCKY

Giesting & Associates
Versailles
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Fax: (606) 873-6233

MARYLAND/VIRGINIA

New Era Sales, Inc.
Severna Park
Tel: (410) 544-4100
Fax: (410) 544-6092

MASSACHUSETTS

Advanced Tech Sales, Inc.
North Reading
Tel: (508) 664-0888
Fax: (508) 664-5503

MICHIGAN

Giesting & Associates
Comstock Park
Tel: (616) 784-9437
Fax: (616) 784-9438

Giesting & Associates
Livonia
Tel: (313) 478-8106
Fax: (313) 477-6908

MINNESOTA

OHMS Technology, Inc.
Edina
Tel: (612) 932-2920
Fax: (612) 932-2918

MISSOURI

Rush & West Associates
St. Louis
Tel: (314) 965-3322
Fax: (314) 965-3529

NEW JERSEY

Strategic Sales, Inc.
Teaneck
Tel: (201) 833-0099
Fax: (201) 833-0061

BGR Associates
Marlton, NJ
Tel: (609) 983-1020
Fax: (609) 983-1879

NEW MEXICO

S & S Technologies
Albuquerque
Tel: (505) 298-7177
Fax: (505) 298-2004

NEW YORK

Strategic Sales, Inc.
New York City
Tel: (201) 833-0099
Fax: (201) 833-0061

Tri-Tech Electronics, Inc.
East Rochester
Tel: (716) 385-6500
Twx: 62934993
Fax. (716) 385-7655

Tri-Tech Electronics, Inc.
Fayetteville
Tel: (315) 446-2881
Twx: 7105410604
Fax: (315) 446-3047

Tri-Tech Electronics, Inc.
Fishkill
Tel: (914) 897-5611
Twx: 62906505
Fax: (914) 897-5611

NORTH CAROLINA

Rep, Inc.
Morrisville
Tel: (919) 469-9997
Fax: (919) 481-3879

OHIO

Giesting & Associates
Cincinnati
Tel: (513) 385-1105
Fax: (513) 385-5069

Giesting & Associates
Cleveland
Tel: (216) 261-9705
Fax: (216) 261-5624

Giesting & Associates
Columbus
Tel: (614) 459-4800
Fax: (614) 459-4801

OKLAHOMA

Bravo Sales, Inc.
Dallas
Tel: (214) 250-2900
Fax: (214) 250-2905

OREGON

Thorson Company
Northwest
Portland
Tel: (503) 293-9001
Fax: (503) 293-9007

PENNSYLVANIA

Giesting & Associates
Pittsburgh
Tel: (412) 828-3553
Fax: (412) 828-6160

BGR Associates
Marlton, NJ
Tel: (609) 983-1020
Fax: (609) 983-1879

PUERTO RICO

QXi of Florida, Inc
Fort Lauderdale
Tel: (305) 978-0120
Fax: (305) 972-1408

TENNESSEE

Rep. Inc.
Jefferson City
Tel: (615) 475-9012
Fax: (615) 475-6340

TEXAS

Bravo Sales, Inc.
Austin
Tel: (512) 836-8323
Fax: (512) 836-1695

Bravo Sales, Inc.
Dallas
Tel: (214) 250-2900
Fax: (214) 250-2905

Bravo Sales, Inc.
Tomball
Tel: (713) 320-0500
Fax: (713) 320-0212

Domestic Representatives (Cont.)

UTAH

Utah Component Sales Inc.
Midvale
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Fax: (801) 561-6016

WASHINGTON

Thorson Company Northwest
Bellevue
Tel: (206) 455-9180
Twx: 9104432300
Fax: (206) 455-9185

WISCONSIN

Victory Sales
Milwaukee
Tel: (414) 789-5770
Fax: (414) 789-5760

OHMS Technology, Inc.
Edina, MN
Tel: (612) 932-2920
Fax: (612) 932-2918

Domestic Distributors

ALABAMA

Arrow/Schweber
Huntsville
Tel: (205) 837-6955
Fax: (205) 721-1581

Time Electronics
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Tel: (205) 721-1133

ARIZONA

Arrow/Schweber
Tempe
Tel: (602) 431-0030
Fax: (602) 431-9555

Insight
Tempe
Tel: (602) 829-1800

Time Electronics
Tempe
Tel: (602) 829-1800

Wyle Laboratories
Phoenix
Tel: (602) 437-2088

CALIFORNIA

Arrow/Schweber
Calabasas
Tel: (818) 880-9686

Arrow/Schweber
San Diego
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Arrow/Schweber
San Jose
Tel: (408) 441-9700

Arrow/Schweber
San Jose
Tel: (408) 432-7171

Arrow/Schweber
Tustin
Tel: (714) 838-5422

Avnet, Inc.
Hughes Aircraft Service Center
Costa Mesa
Tel: (800) 422-8636
Fax: (714) 754-6019

F/X Electronics
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Tel: (818) 591-9220

Insight
San Diego
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Insight
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Tel: (818) 707-2101

Insight
Irvine
Tel: (714) 727-3291

Insight
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Time Electronics
Anaheim
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Time Electronics
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Time Electronics
San Diego
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Time Electronics
Sunnyvale
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Time Electronics
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Wyle Laboratories
Santa Clara
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Wyle Laboratories
Rancho Cordova
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Wyle Laboratories
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Wyle Laboratories
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Wyle Laboratories
San Diego
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Arrow/Schweber
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Arrow/Schweber
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Arrow/Schweber
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Fax: (303) 799-0730

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Fax: (203) 265-7988

Time Electronics
Tel: (203) 271-3200

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Deerfield Beach
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Fax: (305) 428-3991

Arrow/Schweber
Lake Mary
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Time Electronics
Tel: (305) 484-7778

Time Electronics
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Vantage Components
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Vantage Components
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Itasca
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Fax: (201) 984-8908

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Schaumburg
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Schaumburg
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Indianapolis
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Fax: (317) 299-2379

Time Electronics
Tel: (800) 331-5114

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Cedar Rapids
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Fax: (319) 395-0185

Time Electronics
Tel: (800) 325-9085

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Tel: (800) 331-5114

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Columbia
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Fax: (301) 596-7821

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or: (301) 621-8555

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Fax: (313) 462-2686

Time Electronics
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Fax: (612) 941-9405

Arrow/Schweber
Eden Prairie
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Fax: (314) 567-1164

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Time Electronics
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Fax: (609) 596-9632

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Arrow/Schweber
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Fax: (516) 231-1072

Arrow/Schweber
Rochester
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Fax: (716) 427-0735

Time Electronics
Hauppauge (NYC)
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Time Electronics
East Syracuse
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Time Electronics
Rochester
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Vantage Components
Smithtown
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NORTH CAROLINA

Arrow/Schweber
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NORTH DAKOTA

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Fax: (216) 248-1106

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Fax: (513) 435-2049

Time Electronics
Columbus
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Arrow/Schweber
Tulsa
Tel: (918) 252-7537
Fax: (918) 254-0917

OREGON

Almac/Arrow Electronics
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Fax: (503) 645-0611

Insight
Portland
Tel: (503) 644-3300

Time Electronics
Portland
Tel: (503) 684-3780

Wyle Laboratories
Beaverton
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Arrow/Schweber
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Fax: (412) 963-1573

Time Electronics
Philadelphia
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Time Electronics
Pittsburgh
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Time Electronics
Marlton, NJ
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SOUTH DAKOTA

Time Electronics
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Arrow/Schweber
Carrollton
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Fax: (214) 248-7208

Arrow/Schweber
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Tel: (713) 530-4700
Fax: (713) 568-8518

Insight
Austin
Tel: (512) 331-5887

Insight
Houston
Tel: (713) 448-0800

Insight
Richardson
Tel: (214) 783-0800

Time Electronics
Austin
Tel: (512) 339-3051

Time Electronics
Houston
Tel: (713) 530-0800

Time Electronics
Richardson
Tel: (214) 241-7441

Wyle Laboratories
Austin
Tel: (512) 345-8853

Wyle Laboratories
Houston
Tel: (713) 879-9953

Wyle Laboratories
Richardson
Tel: (214) 235-9953

UTAH

Arrow/Schweber
Salt Lake City
Tel: (801) 973-6913
Fax: (801) 972-0200

Time Electronics
West Valley
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Wyle Laboratories
West Valley
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WASHINGTON

Almac/Arrow Electronics
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Fax: (206) 643-9709

Almac/Arrow Electronics
Spokane
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Fax: (509) 928-6096

Insight
Kirkland
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Time Electronics
Redmond
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Wyle Laboratories
Redmond
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WISCONSIN

Arrow/Schweber
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Fax: (414) 792-0156

Marsh Electronics
Milwaukee
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Time Electronics
Tel: (800) 331-5114

International Distributors

AUSTRALIA
GEC/George Brown
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Tel: 61-2-638-1888
Fax: 61-2-638-1798

AUSTRIA
Eljapex
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A-1232 Wein
Tel: (43) 222-86-15-31
Fax: (43) 222-86-15-31-200

BELGIUM, LUX
D&D Electronics bvba
Antwerp
Tel: 32-38277934
Fax: 32-38287254

DENMARK
C-88 A/S
101 Kokkedal Industripark
DK-2980 Kokkedal
Tel: 45-42-24-48-88
Fax: 45-42-24-48-89

UNITED KINGDOM
Micro Call, Ltd.
Thame, Oxon 0X9 3XD
Tel: 44-84-426-1939
Fax: 44-84-426-1678

Silicon Concepts, Ltd.
Hampshire, England
GU30 7SB
Tel: 44-428-751-617
Fax: 44-428-751-603

FINLAND
Nortec Electronics OY
SF-00210 Helsinki
Tel: 358-067-02-77
Tlx: 857125876
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FRANCE
A2M
B.P. 89
78152 LE CHESNAY
CEDEX
Tel: 33 (1) 39-54-91-13
Tlx: 698376F
Fax: 33 (1) 39-54-30-61

Microel
BP3
91941 Les Ulis
CEDEX
Tel: 33 (1) 69-07-08-24
Tlx: 692493F
Fax: 33 (1) 69-07-17-23

GERMANY
Jermyn GmbH
6250 Limburg
Tel: (06) 431-5080
Fax: (06) 431-508289

Scantec GmbH
D-33 Planegg
Tel: (089) 859-8021
Tlx: 5213219
Fax: (089) 857-6574

Topas Electronic GmbH
3000 Hannover 1
Tel: (0511) 13-12 -17
Tlx: 9218176
Fax: (0511) 13-12-16

HOLLAND
Arcobel bv
Griekenweg 25
5342 Px OSS
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Fax: 31-4120-30635

HONG KONG
CET, Ltd.
Tel: 852-520-0922
Fax: 852-865-0639

INDIA/PAKISTAN/BRAZIL
Pamir Electronics Corp.
400 West Lancaster
Devon, PA 19333 USA
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Fax: 215-688-5382
Tlx: 210656 Pamir UR

ISRAEL
Vectronics
60 Medinat Hayehudim St.
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Herzlia B 46120, Israel
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ITALY
Comprel s.p.a.
20092 Cinisello B.
Milano
Tel: (02) 6120641/5
Tlx: 332484 COMPRL
Fax: (02) 6128158

Silverstar
20126 Milano
Tel: 39 2661251
Fax: 39 266101922

JAPAN
Internix, Inc.
Shinjuku Hamada
Bldg. 7-4-7
Nishi-Shinjuku, Shinjuku-Ku
Tokyo 160
Tel: 813-3-369-1105
Fax: 813-3-363-8486

Kyocera Corporation
Setagaya-ku, Tokyo
Tel: 813-3-708-3111
Tlx: 7812466091
Fax: 813-3-708-3864

Nippon Imex Corporation
Setagaya-ku, Tokyo
Tel: 813-3-321-8000
Tlx: 78123444
Fax: 813-3-325-0021

KOREA
Eastern Electronics, Inc.
Kangnam-Gu, Seoul
Tel: 82-2-553-2997
Tlx: 78727381
Fax: 82-2-553-2998

NORWAY
Nortec Electronics A/S
Postboks 123
N-1364 Hvalstad
Tel: 2-84-62-10
Fax: 2-84-65-45

PORTUGAL
ATD Electronica, Lda.
Rua Faria de
Vasconcelos, 3-A
1900 Lisboa
Tel: 3511-847-2200
Fax: 3511-847-2197

SINGAPORE
Westech Electronics
Singapore 1334
Tel: 65-743-6355
Tlx: RS 55070
WESTEC
Fax: 65-746-1396

SPAIN
Sagitron
Corazon de Maria 80
28002 Madrid
Tel: 416-92-61
Tlx: 43819
Fax: 415-86-52

SWEDEN
Nortec Electronics A/B
Box 1830
S-171 27 Solna
Tel: 8-7051800
Fax: 8-836918

SWITZERLAND
Eljapex
Hardstr. 72
CH - 5430 Wettingen
Tel: (41) 56-27-57-77
Fax: (41) 56-26-14-86

Laser & Electronic
Equipment
8053 Zurich
Tel: 41 (1) 55-33-30
Fax: 41 (1) 55-34-58

TAIWAN
Ally, Inc.
Taipei
Tel: 886-2-788-6270
Fax: 886-2-786-3550

WSI Direct Sales Offices

REGIONAL SALES

Midwest
Hoffman Estates, IL
Tel: (708) 882-1893
Fax: (708) 882-1881

Southwest
Irvine, CA
Tel: (714) 753-1180
Fax: (714) 753-1179

Mid-Atlantic
Trevose, PA
Tel: (215) 638-9617
Fax: (215) 638-7326

Southeast
Dallas, TX
Tel: (214) 680-0077
Fax: (214) 680-0280

Northwest
Fremont, CA
Tel: (510) 656-5400
Telex: 289255
Fax: (510) 657-5916

EUROPE SALES

WSI – France
2 voie LA CARDON
91126 PALAISEAU
CEDEX, France
Tel: 33 (1) 69-32-01-20
Fax: 33 (1) 69-32-02-19

WSI – Germany
c/o B&RS
Rosenstrasse 7
8000 Munich 2, Germany
Tel: (49) 89.23.11.38.49
Fax: (49) 89.23.11.38.11

ASIA SALES

WSI – Asia, Ltd.
1006 C.C. Wu Bldg.
302-308 Hennessy Road
Wan Chai, Hong Kong
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Fax: 852-893-0678

Corporate Headquarters

47280 Kato Road
Fremont, California 94538-7333
Tel: 510-656-5400 Fax: 510-657-5916
Telex: 289255
800-TEAM-WSI (800-832-6974)
In California 800-562-6363

LIFE SUPPORT POLICY:

WaferScale Integration, Inc. (WSI) products are not authorized for use as critical components in life support systems or devices without the express written approval of the President of WSI. As used herein:

A) Life support devices or systems are devices or systems which 1) are intended for surgical implant into the body, or 2) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury or death to the user.

B) A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.
